



**User Manual**

# **SOM-7533**

## **CPU Computer on Module**

**ADVANTECH**

*Enabling an Intelligent Planet*

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Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

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If you believe your product to be defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

# Declaration of Conformity

## CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

Test conditions for passing also include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

## FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

## FM

This equipment has passed FM certification. According to the National Fire Protection Association, work sites are categorized into different classes, divisions, and groups based on hazard considerations. This equipment is compliant with the specifications for Class I, Division 2, Groups A, B, C, and D indoor hazards.

# Technical Support and Assistance

1. Visit the Advantech website at [www.advantech.com/support](http://www.advantech.com/support) to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
  - Product name and serial number
  - Description of your peripheral attachments
  - Description of your software (operating system, version, application software, etc.)
  - A complete description of the problem
  - The exact wording of any error messages

---

## Warnings, Cautions, and Notes

**Warning!** Warnings indicate conditions that could cause personal injury if not observed!



**Caution!** Cautions are included to help prevent hardware damage and data loss. For example,



*“Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer’s instructions.”*

**Note!** Notes provide additional and/or optional information.



## Document Feedback

To assist us with improving this manual, we welcome all comments and constructive criticism. Please send all feedback in writing to [support@advantech.com](mailto:support@advantech.com).

## Safety Precautions - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.
- Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

# Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from all power outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If any of the following occurs, have the equipment checked by service personnel:
  - The power cord or plug is damaged.
  - Liquid has penetrated the equipment.
  - The equipment has been exposed to moisture.
  - The equipment is malfunctioning, or does not operate according to the user manual.
  - The equipment has been dropped and damaged.
  - The equipment shows obvious signs of breakage.
15. Do not leave the equipment in an environment with a storage temperature of below  $-20^{\circ}\text{C}$  ( $-4^{\circ}\text{F}$ ) or above  $60^{\circ}\text{C}$  ( $140^{\circ}\text{F}$ ) as this may damage the components. The equipment should be kept in a controlled environment.
16. **CAUTION:** Batteries are at risk of exploding if incorrectly replaced. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
17. In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator's position should not exceed 70 dB (A).

**DISCLAIMER:** This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.



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# Chapter 1

## General Information

This chapter gives background information on the SOM-7533 CPU Computer on Module.

Sections include:

- Introduction
- Functional Block Diagram
- Product Specifications

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## 1.1 Introduction

SOM-7533 is a COM Express Compact module with pin-out Type 10 that fully complies with the PICMG (PCI Industrial Computer Manufacturers Group) COM R3.1 specifications. The CPU module utilizes Intel® i3 & N-series and Atom® x7000E Series Processors (formally called Alder Lake N) in a mini-sized 55x84mm COM Express form factor, featuring a 15-watt thermal design power (TDP) rating.

Compared with previous platforms, SOM-7533 has 1.4X better CPU and 2X better graphics performance. It supports up to 16GB single-channel LPDDR5 4800MT/s memory. In addition, there are numerous high-speed I/O interfaces included, such as PCIe Gen3 (8.0GT/s) and 2.5Gbase-T, USB 3.2 Gen 2 (10Gbps), and CAN-FD for abundant system expandability. Moreover, it can be connected to two independent displays up to 4K. Available connections include DisplayPort 1.4, HDMI 2.0, and one optional eDP or LVDS. It also features optional eMMC and onboard TPM 2.0 with 4.75~20V power input. SOM-7533 is a reliable and suitable solution for industrial and automation needs.

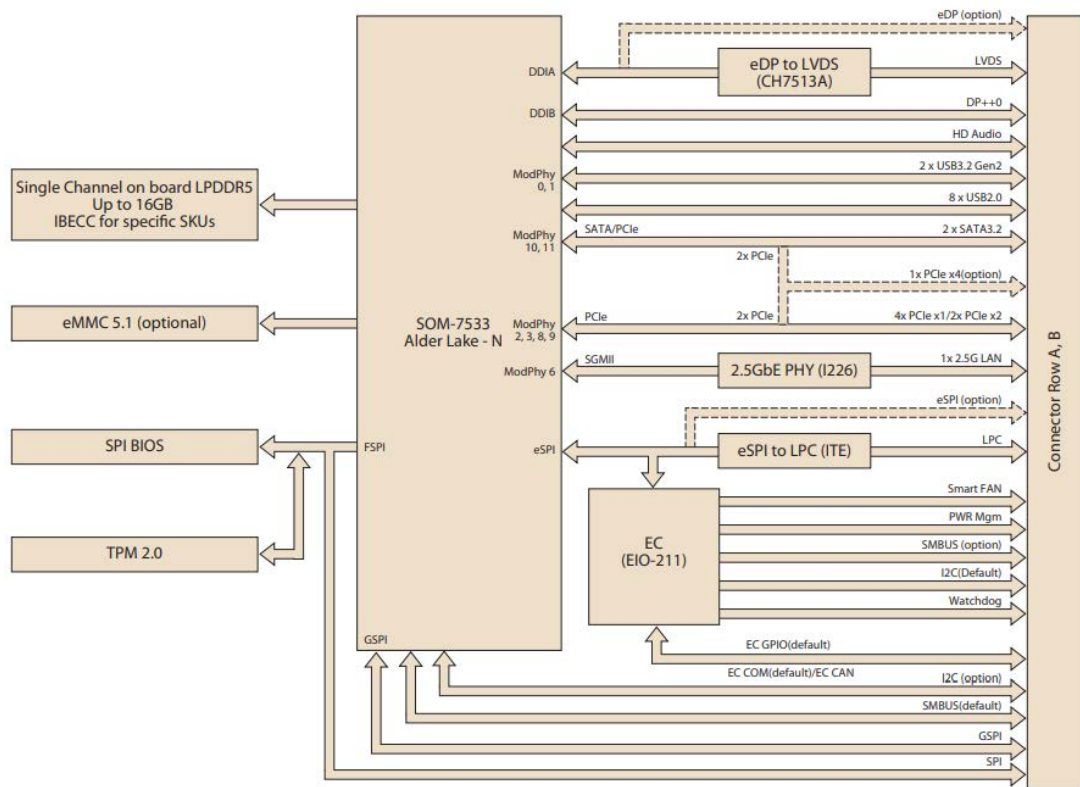
Advantech iManager (SUSI 4) was created to meet the needs of embedded applications. It offers features including a multi-level watchdog timer, monitoring of voltage and temperature, thermal protection and mitigation through processor throttling, LCD backlight on/off and brightness control, embedded storage for customized information, and more. When paired with Advantech WISE-PaaS/RMM, it enables remote monitoring and control of devices over the Internet, simplifying maintenance tasks. Every Advantech module comes with iManager and WISE-PaaS/RMM integrated, providing enhanced value for customer applications.

SOM-7533 is designed to excel even in extreme conditions, offering low power consumption and a variety of expansion I/O interfaces. It's a computing-centric product with advanced thermal management, making it ideal for tasks heavy on graphics, media, and demanding I/O applications.

**Table 1.1: Acronyms**

<b>Term</b>	<b>Define</b>
AC'97	Audio CODEC (Coder-Decoder)
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PC-AT systems
BIOS	Basic Input Output System – firmware in a PC-AT system that is used to initialize system components before handing control over to the operating system
CAN	Controller-area network (CAN or CAN-bus) is a vehicle bus standard designed to allow micro-controllers to communicate with each other within a vehicle without a host computer
DDI	Digital Display Interface – containing DisplayPort, HDMI/DVI, and SDVO
EAPI	Embedded Application Programmable Interface Software interface for COM Express <sup>®</sup> specific industrial functions <ul style="list-style-type: none"> <li>– System information</li> <li>– Watchdog timer</li> <li>– I<sup>2</sup>C Bus</li> <li>– Flat-panel brightness control</li> <li>– User storage area</li> <li>– GPIO</li> </ul>
GbE	Gigabit Ethernet
GPIO	General purpose input output
HDA	Intel <sup>®</sup> High Definition Audio (HD Audio) refers to the specification released by Intel in 2004 for delivering high definition audio that is capable of playing back more channels at higher quality than AC'97.
I <sup>2</sup> C	Inter Integrated Circuit – 2-wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values
ME	Management Engine
PC-AT	“Personal Computer – Advanced Technology” – an IBM trademark term used to refer to Intel-based personal computers in the 1990s
PEG	PCI Express Graphics
RTC	Real-Time Clock – battery-backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
SPD	Serial Presence Detect – refers to serial EEPROM on DRAM that has DRAM Module configuration information
TPM	Trusted Platform Module, chip to enhance the security features of a computer system
UEFI	Unified Extensible Firmware Interface
WDT	Watchdog Timer

## 1.2 Functional Block Diagram



## 1.3 Product Specifications

### 1.3.1 Compliance

- PICMG COM.0 (COM Express) Revision 3.1
- Mini Size - 55 x 84 mm
- Pin-out Type 10 compatible

### 1.3.2 Feature List

**Table 1.2: Feature List**

Feature Type	Connector Row	Feature	Type 10 Definition		SOM-7533
			Max.	Min.	
Display	A-B	LVDS Channel A (18-/24-bit)	1	0	1
	A-B	eDP (muxed on LVDS Channel A)	1	0	1
Expansion	A-B	PCI Express x1	4	1	4
	A-B	LPC	1	1	1
Serial	A-B	SMBus	1	1	1
	A-B	I <sup>2</sup> C Bus	1	1	1
	A-B	Serial Port	2	0	2
	A-B	CAN BUS (muxed on SER1)	1	0	1
I/O	A-B	LAN Port 0 (Gigabit Ethernet)	1	1	1
	A-B	SATA	2	1	2
	A-B	USB 2.0	8	4	8
	A-B	USB Client	2	0	2
	A-B	HD Audio	1	0	1
	A-B	SPI Bus	2	1	1
	A-B	General Purpose I/O (GPIO)	8	8	8
	A-B	Watchdog Timer Output	1	0	1
	A-B	Speaker Out	1	1	1
	A-B	External BIOS ROM Support	1	0	1+1
	A-B	Power Button Support	1	1	1
	A-B	Power Good	1	1	1
	A-B	VCC_5V_SBY Contacts	4	4	4
	A-B	Sleep	1	0	1
	A-B	Thermal Protection	1	0	1
	A-B	Lid Input	1	0	1
	A-B	Battery Low Alarm	1	0	1
	A-B	Suspend/Wake Signals	3	0	3
	A-B	Fan PWM/Tachometer	2	0	1
	A-B	Trusted Platform Modules	1	0	1
	A-B	USB 3.0	2	0	2

### 1.3.3 Processor System

**Table 1.3: Processor System**

CPU	Std. Freq.	Max. Turbo Freq.	Core	Cache (MB)	TDP(W)
I3-N305	1.0/1.8 GHz	3.8 GHz	8	6	9/15W
N97	2.0 GHz	2.9 GHz	4	6	12W
N200	1.0 GHz	3.2 GHz	4	6	6W
N50	1.0 GHz	3.4 GHz	2	6	6W
Atom x7425E	1.5 GHz	2.7 GHz	4	6	12W

### 1.3.4 Memory

Single channels, onboard LPDDR5 4800MT/s up to 16GB.

### 1.3.5 Graphics/Audio

Graphics Core: Intel® UHD Graphics for 12th Gen Intel® Processors supporting AVC, MPEG-2, HEVC, and VP9 DX12.1, OGL4.6, OCL3.0, and MPEG2, HEVC/H265, VC1/WMV9 HW decode/encode/transcode acceleration.

**Table 1.4: Graphics/Audio**

CPU	Graphics Core	Base Freq.	Max Freq.
I3-N305	Gen12 UHD Graphics	1.0GHz	1.25GHz
N97	Gen12 UHD Graphics	850MHz	1.20GHz
N200	Gen12 UHD Graphics	450MHz	750MHz
N50	Gen12 UHD Graphics	600MHz	750MHz
Atom x7425E	Gen12 UHD Graphics	800MHz	1.00GHz

### 1.3.6 Expansion Interface

#### 1.3.6.1 PCIe x1

PCI Express x1: Supported by default: 4 x PCIe x1 compliant with PCIe Gen3 (8.0 GT/s) specifications, configurable to PCIe x4 or PCIe x2. Several configurable combinations may need BIOS modification. Please contact the Advantech sales or FAE for more details.

**Table 1.5: PCIe x1**

Type 10	Row A,B			
	P0	P1	P2	P3
Default	X1	X1	X1	X1
Option 1	X4			

#### 1.3.6.2 LPC

Supports the Low Pin Count (LPC) 1.1 specification, without DMA or bus mastering. It enables connection to Super I/O, an embedded controller, or TPM; 24MHz LPC clock.



## 1.3.7 Serial Bus

### 1.3.7.1 SMBus

Supports the SMBus 2.0 specification.

### 1.3.7.2 I<sup>2</sup>C Bus

Supports I<sup>2</sup>C bus, 7-bit and 10-bit address modes. It supports standard mode up to 100 Kb/s and fast mode up to 400 Kb/s.

## 1.3.8 I/O

### 1.3.8.1 Gigabit Ethernet

Ethernet: Intel® I226 Gigabit LAN supports 10/100/1000 Mbps & 2.5 Gbps speed.

### 1.3.8.2 SATA

Supports 2 x SATA Gen3 (6.0 Gb/s), backward compatible with SATA Gen2 (3.0 Gb/s) and Gen1 (1.5 Gb/s). The maximum data rate is 600 MB/s. It supports AHCI 1.3.1 mode (and does not support IDE mode).

### 1.3.8.3 USB 3.2 / USB 2.0

SOM-7533 supports 2 x USB 3.2 Gen 2 (10 Gbps) and 8 x USB 2.0 (480 Mbps) which are reverse compatible to USB 1.x. For USB 3.2, the product supports LPM (U0, U1, U2, and U3) for power efficiency.

Notice: To meet USB 3.2 Gen 2 performance, Advantech strongly recommends using a certified cable.

### 1.3.8.4 USB 3.2

**Table 1.6: USB 3.2**

Type 10	P0	P1
SoC	P0	P1
Type 10	OC_01	
SoC USB_OC#	OC_0	

### 1.3.8.5 USB 2.0

**Table 1.7: USB 2.0**

<b>Type 10</b>	P0	P1	P2	P3	P4	P5	P6	P7
<b>SoC</b>	P0	P1	P2	P3	P4	P5	P6	P7
<b>Type 10</b>	OC_01		OC_23		OC_45		OC_67	
<b>SoC USB_OC#</b>	OC_0		OC_2		OC_3		OC_1	

### 1.3.8.6 SPI Bus

Supports BIOS flash only. The SPI clock can be 20MHz, with capacity up to 256Mb.

### 1.3.8.7 GPIO

8 x programmable general purpose input or output (GPIO).

### 1.3.8.8 Watchdog Timer

There is support for multi-level watchdog time-out output. 1-65535 levels, from 100 ms to 109.22 minute intervals.

### 1.3.8.9 Serial Ports

2 x 2-wire serial ports (Tx/Rx) support 16550 UART compliance:

- Programmable FIFO or character mode
- 16-byte FIFO buffer on the transmitter and receiver in FIFO mode
- Programmable serial-interface characteristics: 5-, 6-, 7-, or 8-bit character
- Even, odd, or no parity bit selectable
- 1, 1.5, or 2 stop bits selectable
- Baud rate up to 115.2K

### 1.3.8.10 TPM

Supports optional TPM 2.0 module.

### 1.3.8.11 Smart Fan

Supports 1 Fan PWM control signal and 1 tachometer input for fan speed detection. There is support for 1 on the carrier board following PICMG COM Express R3.1 specifications.

### 1.3.8.12 BIOS

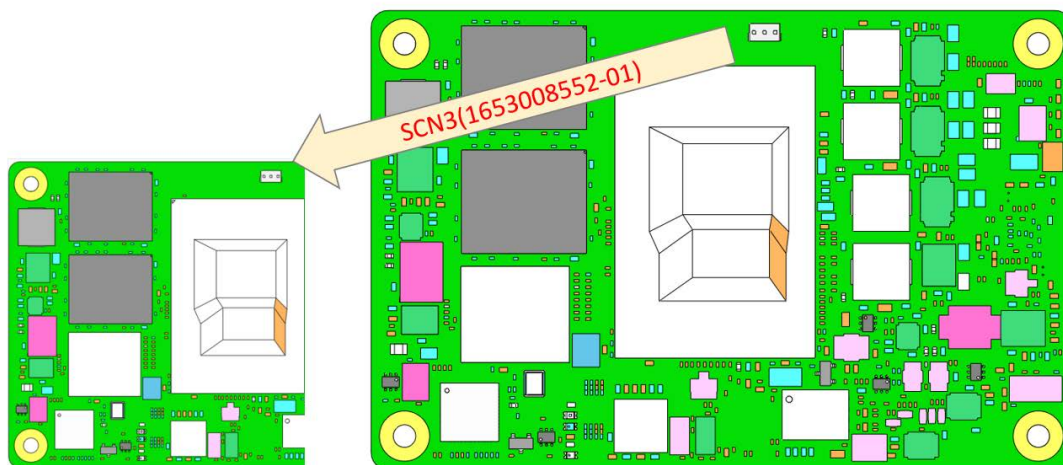
The BIOS chip is on the module by default. Users can place the BIOS chip on the carrier board with appropriate design and jumper settings in BIOS\_DIS#[1:0].

**Table 1.8: BIOS**

BIOS_DIS#0	BIOS_DIS#1	Bootup Destination/Function
Open	Open	Boot from Module SPI BIOS
Open	GND	SPI_CS0# to Carrier Board, SPI_CS1# to Module
GND	GND	SPI_CS0# to Module, SPI_CS1# to Carrier Board

**Note: If system COMS is cleared, Advantech strongly suggests going to the BIOS setup menu and loading default settings on the first bootup.**

The standard module has no jumper at SCN3, so BIOS settings are kept without an RTC coin battery. If you need to restore BIOS default settings, follow the steps below:



1. Remove the coin battery.
2. Put the jumper on SCN3 pins 1-2.
3. Turn on the power supply.
4. The system will boot up a few times.
5. The BIOS will load the default settings.

## 1.3.9 Power Management

### 1.3.9.1 Power Supply

There is support for both ATX and AT power modes. VSB is for suspended power and is optional if not required by standby (suspend-to-RAM). An RTC battery is optional if date/timekeeping is not required.

- VCC: 4.75V (5V-5%) – 20V (19V+5%)
- VSB: 5V ± 5% (suspend power)
- RTC Battery Power: 2.0V – 3.3V

### 1.3.9.2 PWROK

Power OK from the main power supply. A high value indicates the power level is good. This signal can be used to postpone module startup allowing carrier-based FPGAs or other configurable devices to be programmed.

### 1.3.9.3 Power Sequence

According to PICMG COM Express COM.0 R 3.1 specifications.

### 1.3.9.4 Wake Event

Various wake events are supported to allow users to set it up for different scenarios.

- Wake-on-LAN(WOL): Wake to S0 from S3/S4/S5
- USB Wake: Wake to S0 from S3
- PCIe Device Wake: depends on user inquiry and may need customized BIOS
- LPC Wake: depends on user inquiry and may need customized BIOS

### 1.3.9.5 Advantech S5 ECO Mode (Deep Sleep Mode)

Advantech iManager provides additional features allowing the system to enter a very low suspended power mode – S5 ECO mode. In this mode, the module will cut all power, including suspended and active power to the chipset, and keep an on-module controller active. Only power under 50MW will be consumed, meaning user battery packs can last longer. While this mode is enabled in the BIOS, the system (or module) only allows a power button boot instead of other methods such as WOL.

## 1.3.10 Environment

### 1.3.10.1 Temperature

- **Operating:** 0 ~ 60°C (32 ~ 140°F)
- **Storage:** -40 ~ 85°C (-40 ~ 185°F)

### 1.3.10.2 Humidity

- **Operating:** 40°C @ 95% relative humidity, non-condensing
- **Storage:** 60°C @ 95% relative humidity, non-condensing

### 1.3.10.3 Vibrations

**IEC60068-2-64:** Random vibration test under operation mode, 3.5 Grms.

### 1.3.10.4 Drop Test (Shock)

Federal Standard 101 Method 5007 test procedure with standard packing.

### 1.3.10.5 EMC

CE EN55022 Class B and FCC Certifications: validated with standard development boards in the Advantech chassis.

## 1.3.11 MTBF

Please refer to the Advantech SOM-7533 Refresh Series Reliability Prediction report on the website: <http://com.advantech.com>

## 1.3.12 OS Support

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft Windows Embedded technology." We enable Windows Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows Embedded software solutions easily and widely available to the embedded computing community.

To install drivers, please connect to the website (<http://support.advantech.com.tw>) to download the setup file.

## 1.3.13 Advantech iManager

iManager supports APIs for GPIO, smart fan control, multi-stage watchdog timer, temperature sensor, and hardware monitoring. It follows PICMG EAPI 1.0 specifications with backward compatibility.

### 1.3.14 Power Consumption

**Table 1.9: Power Consumption Table (Watts)**

VCC=12V, VSB=5V	Active Power Domain			Suspend Power Domain		Mechanical off
	Power State	S0 Max. Load	S0 Burn-in	S0 Idle	S5	S5 Deep Sleep
SOM-7533DCCC-S8A1	36.45W	31.37W	4.80W	0.57W	0.59W	4.5uA
SOM-7533CCBC-U0A1	22.84W	16.27W	4.40W	0.59W	0.59W	5.84uA

#### Hardware Configurations:

1. MB: SOM-7533DCCC-S8A1
2. DRAM: 16GB LPDDR5 4800MT/s
3. Carrier board: SOM-DB5830-00A3

#### Test Condition:

1. Test temperature: room temperature (about 25°C)
2. Test voltage: rated voltage DC +12.0V
3. Test loading:
  - Maximum load mode: According to Intel thermal/power test tools.
  - Burn-in mode: Burn-in test V8.1 Pro (1023) for 64-bit Windows (CPU, RAM, 2D&3D Graphics and Disk with 100%).
  - Idle mode: DUT power management off and not running any programs.
4. OS: Windows 10 Enterprise

#### 1.3.14.1 Performance

To compare performance or benchmark data with other modules, please refer to the “Advantech COM Performance & Power Consumption Table.”

### 1.3.15 Selection Guide w/ P/N

**Table 1.10: Selection Guide w/ P/N**

Part No.	CPU	Cores	Graphics	Base Freq.	Max. Boost Freq.	GFX HFM	GFX Burst Mode	Onboard Memory	CPU TDP	eMMC	IBECC	Thermal solution	Operating Temp.
SOM-7533DCC C-S8A1	I3-N305	8	32 EU	1.0GHz/1.8GHz	3.8GHz	1.0GHz	1.25GHz	16G	9W/15W	64G	Yes	Passive	0 ~ 60°C
SOM-7533CCB C-U0A1	N97	4	24 EU	2.0GHz	3.6GHz	850MHz	1.2GHz	8G	12W	32G	Yes	Passive	0 ~ 60°C
SOM-7533DCB C-S0A1	N200	4	32 EU	1.0GHz	3.7GHz	450MHz	750MHz	16G	6W	32G	Yes	Passive	0 ~ 60°C
SOM-7533BCA C-S0A1	N50	2	16 EU	1.0GHz	3.4GHz	600MHz	750MHz	4G	6W	16G	Yes	Passive	0 ~ 60°C
SOM-7533CCB C-S5A1	Atom x7425E	4	24 EU	1.5GHz	3.4GHz	800MHz	1.0GHz	8G	12W	32G	Yes	Passive	0 ~ 60°C

### 1.3.16 Packing list

**Table 1.11: Packing List**

Part No.	Description	Quantity
-	SOM-7533 COM module	1
1970005865T001	Heatspreader	1

### 1.3.17 Development Board

**Table 1.12: Development Board**

Part No.	Description
SOM-DB5830-00A3	COMe Devel. Board COMe R3.1 Type6 pin-out (LVDS) 0 ~ 60°C
SOM-DB5830A-00A3	COMe Devel. Board COMe R3.1 Type6 pin-out (eDP) 0 ~ 60°C

Note: SOM-7533 needs to have the middle board EA00 assembly. Then the pin out will map to Type 10 with SOM-DB5830.

### 1.3.18 Optional Accessory

**Table 1.13: Optional Accessory**

Part No.	Description
1970005864T001	Semi-Heatsink

### 1.3.19 Pin Description

Advantech provides useful checklists for schematic design and layout routing. In the schematic checklist, it will specify details about each pin's electrical properties and how to connect them for different user scenarios. In the layout checklist, it will specify the layout constraints and recommendations for trace length, impedance, and other necessary information during design.

Please contact your nearest Advantech branch office or call to obtain design documents and further advanced support.

# Chapter 2

## Mechanical Information

This chapter gives mechanical information for the SOM-7533 CPU Computer on Module.

Sections include:

- Board Information
- Mechanical Diagrams
- Assembly Diagrams

## 2.1 Board Information

The figures below indicate the main chips on the SOM-7533 Computer-on-Module. Please be aware of these positions when designing a customer's carrier board to avoid mechanical interference and thermal solution contacts for best thermal dissipation performance.

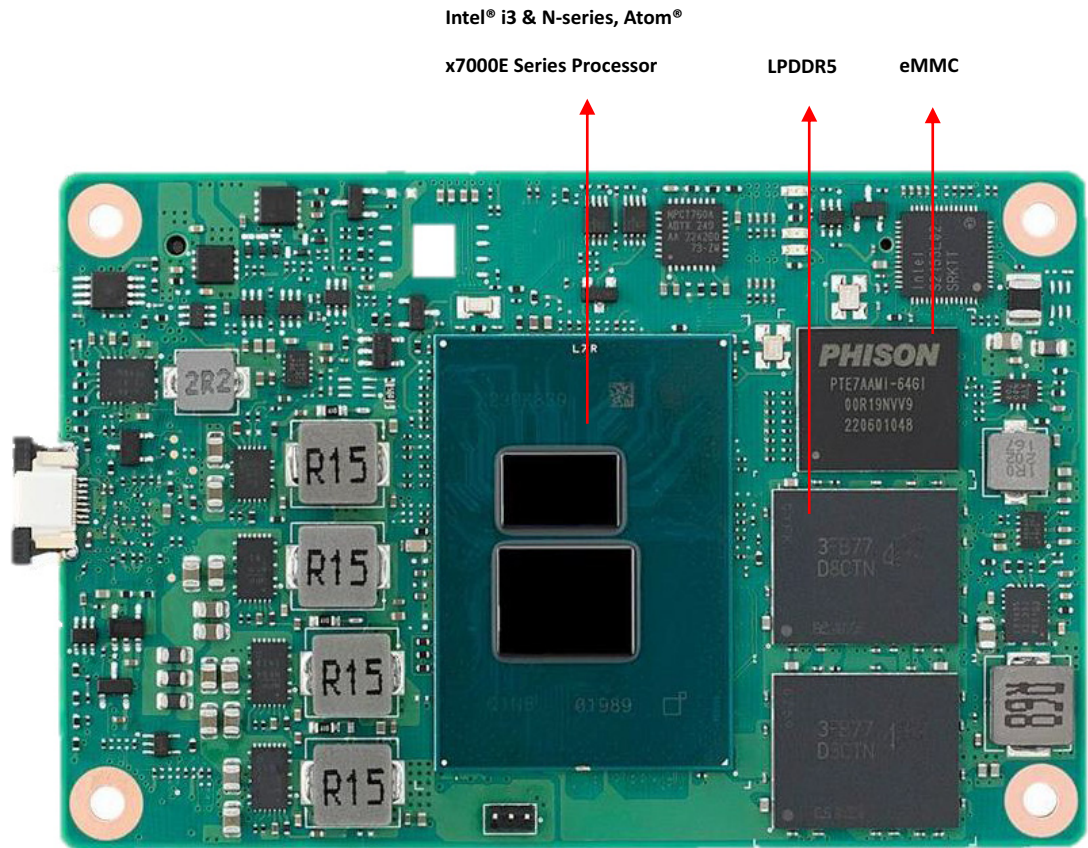


Figure 2.1 Board Chips ID – Front

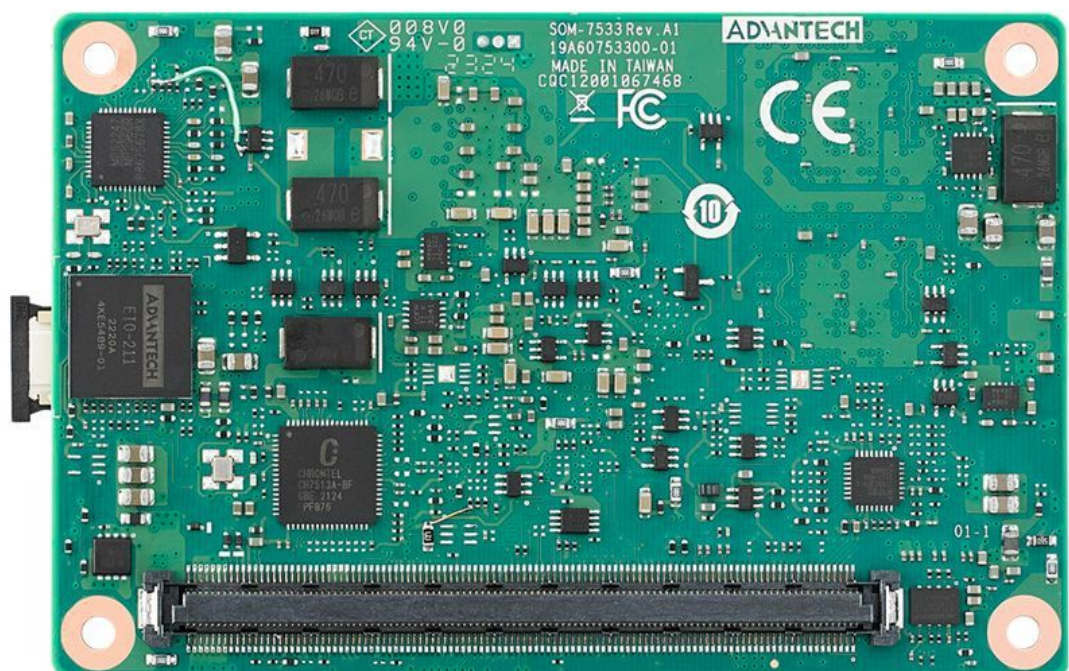


Figure 2.2 Board Chips ID – Rear



## 2.2 Mechanical Diagrams

For more details on 2D/3D models, please find them on the Advantech COM support service website: <http://com.advantech.com>.

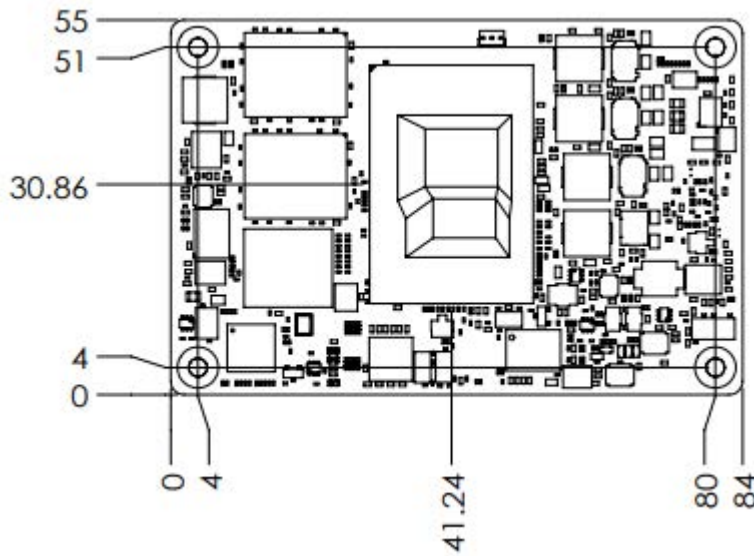


Figure 2.3 Board Mechanical Diagram – Front

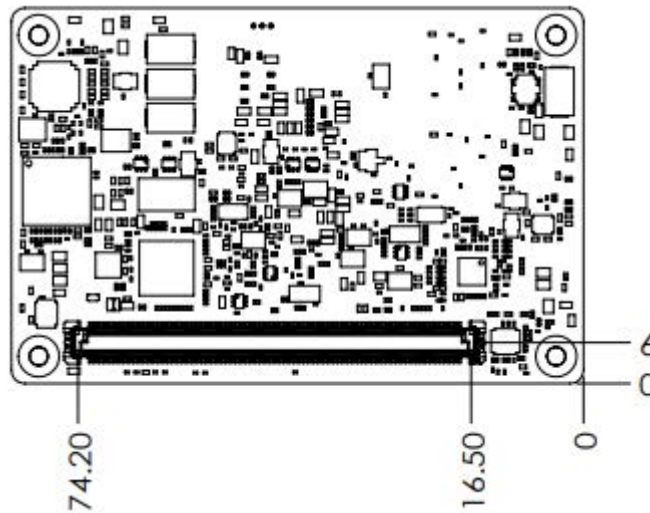


Figure 2.4 Board Mechanical Diagram – Rear

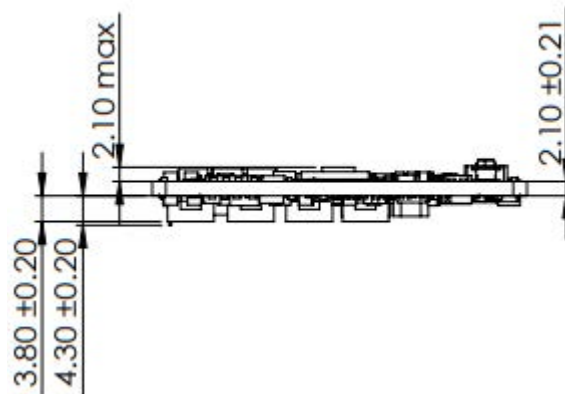
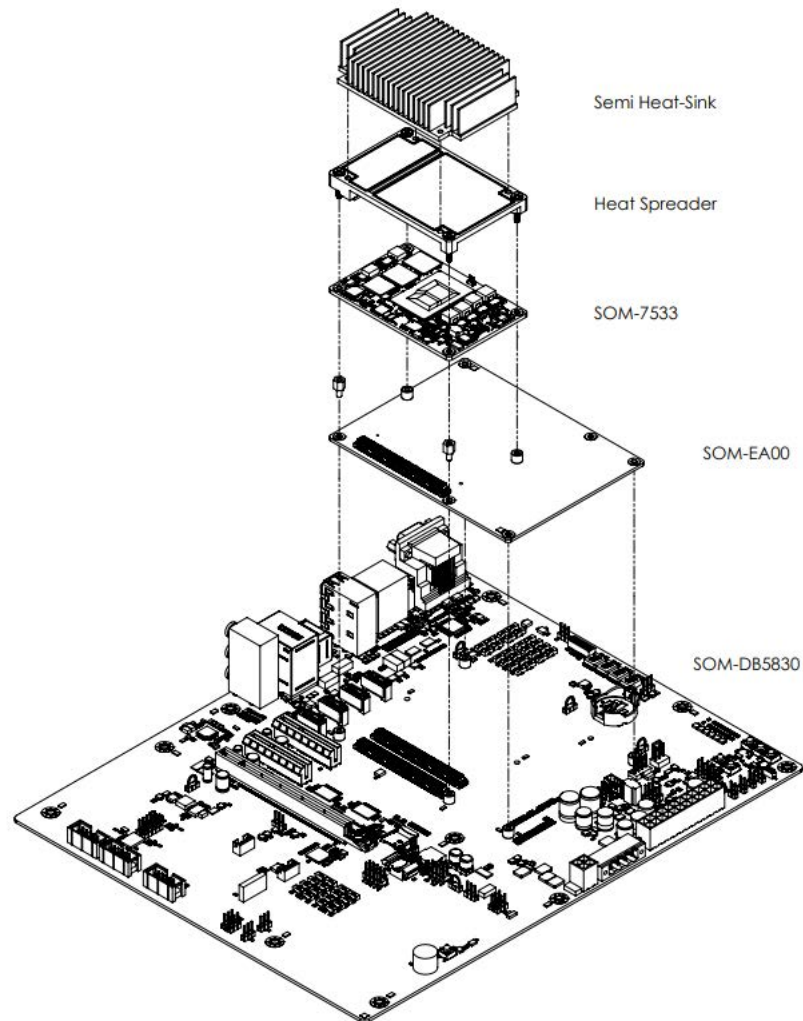


Figure 2.5 Board Mechanical Diagram – Side

## 2.3 Assembly Diagrams

These figures demonstrate the order of assembly for attaching the thermal module and COM module to the carrier board.

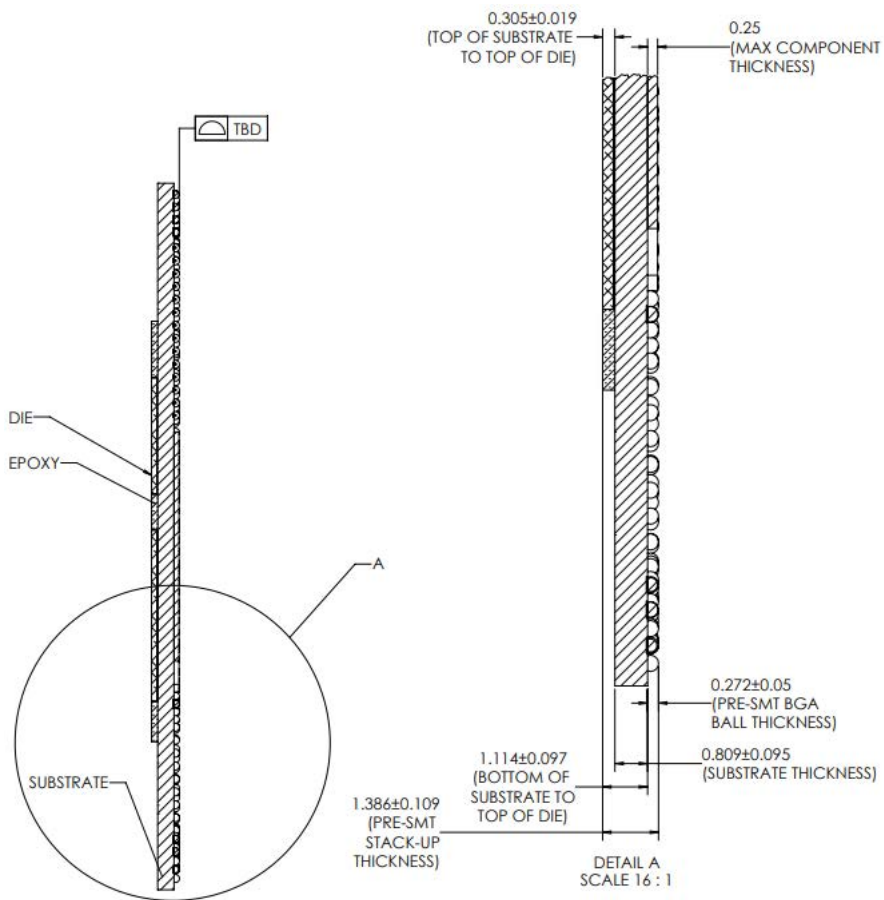


**Figure 2.6 Assembly Diagram**

There are 4 reserved screw holes for SOM-7533 to be pre-assembled with a heat spreader.

## 2.4 Assembly Diagram

Please consider the CPU and chip height tolerance when designing your thermal solution.



**Figure 2.7 CPU Height and Tolerance**



# Chapter 3

## AMI BIOS

This chapter provides BIOS setup information for the SOM-7533 CPU Computer on Module.

Sections include:

- Introduction
- Entering Setup
- Hot/Operation Keys
- Exiting the BIOS Setup Utility

## 3.1 Introduction

AMI BIOS has been integrated into many motherboards for over a decade. With the AMI BIOS Setup Utility, users can modify BIOS settings and control various system features. This chapter describes the basic navigation of the BIOS Setup Utility.



**Figure 3.1 Setup Program Initial Screen**

AMI's BIOS ROM has a built-in setup program that allows users to modify the basic system configuration. This information is stored in flash ROM so it retains the setup information when the power is turned off.

## 3.2 Entering Setup

Turn on the computer and then press <DEL> or <ESC> to enter the Setup menu.

### 3.3 Main Setup

When users first enter the BIOS Setup Utility, users will enter the Main setup screen. Users can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



**Figure 3.2 Main Setup Screen**

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

- **System Time / System Date**

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

## 3.4 Advanced BIOS Features Setup

Select the Advanced tab from the SOM-7533 setup screen to enter the Advanced BIOS Setup screen. Users can select any item in the left frame of the screen, such as CPU Configuration, to go to the sub-menu for that item. Users can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens are shown below. The sub-menus are described on the following pages.

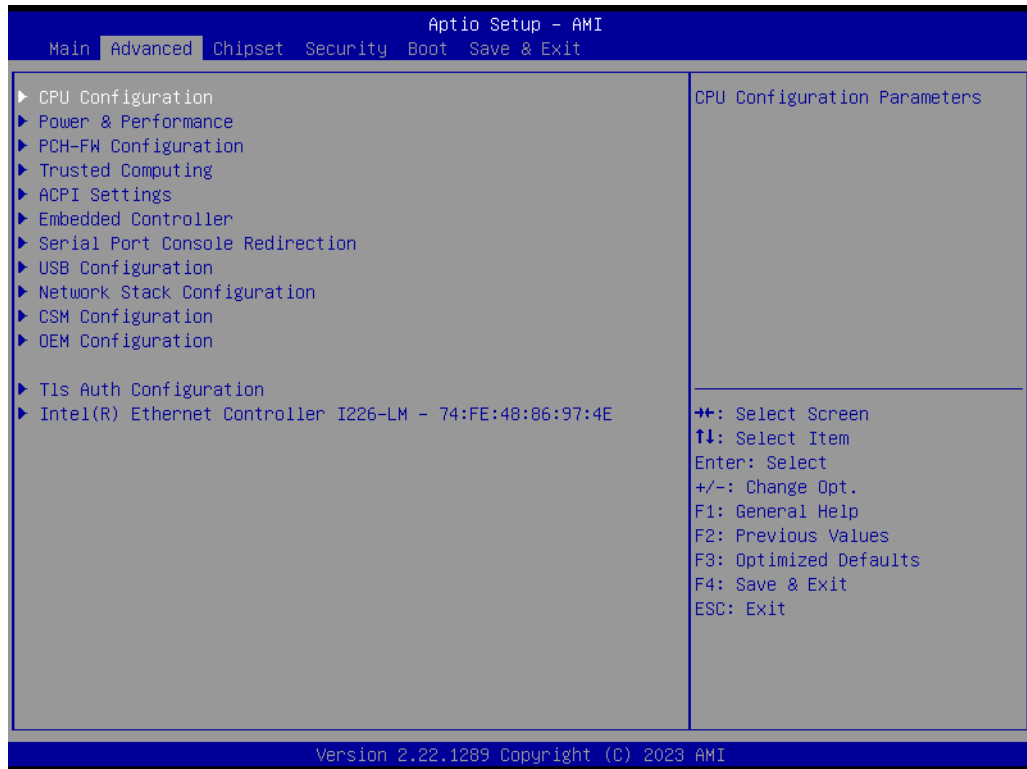


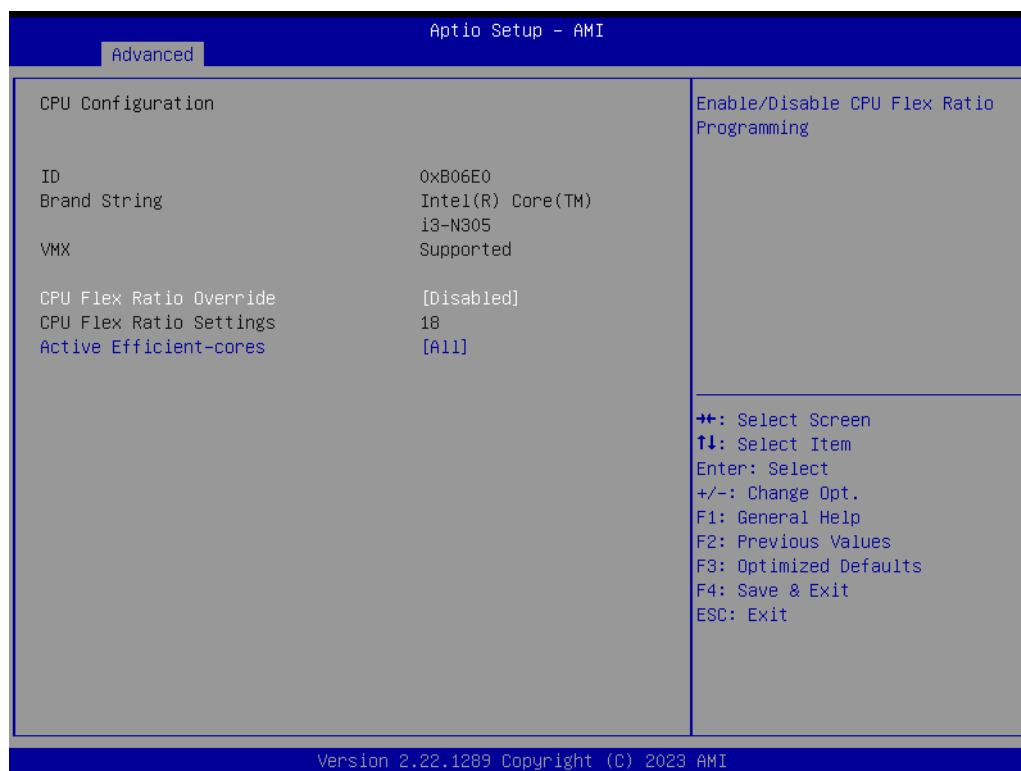
Figure 3.3 Advanced BIOS Features Setup Screen

- **CPU Configuration**  
CPU Configuration Parameters.
- **Power & Performance**  
Power & Performance Options.
- **PCH-FW Configuration**  
Configure Management Engine Technology Parameters.
- **Trusted Computing**  
Trusted Computing Settings.
- **ACPI Settings**  
ACPI Sleep State.
- **Embedded Controller**  
Embedded Controller Parameters.
- **Serial Port Console Redirection**  
Console Redirection Settings.
- **USB Configuration**  
USB Configuration Parameters.
- **Network Stack Configuration**  
Network Stack Settings.
- **CSM Configuration**  
CSM Configuration: Enable/Disable, Option ROM execution settings, etc.



- **OEM Configuration**  
Advanced settings.
- **Tls Auth Configuration**  
Press <Enter> to select Tls Auth Configuration.
- **Intel(R) Ethernet Controller I226-LM-74:FE:48:86:97:4E**  
Configure Gigabit Ethernet device parameters.

### 3.4.1 CPU Configuration



**Figure 3.4 CPU Configuration**

- **CPU Flex Ratio Override**  
Enable/Disable CPU Flex Ratio programming.
- **Active Efficient-cores**  
Numbers of E-cores to enable in each processor package. Note: The number of Cores and E-cores are looked at together. When both are {0,0}, Pcode will enable all cores.

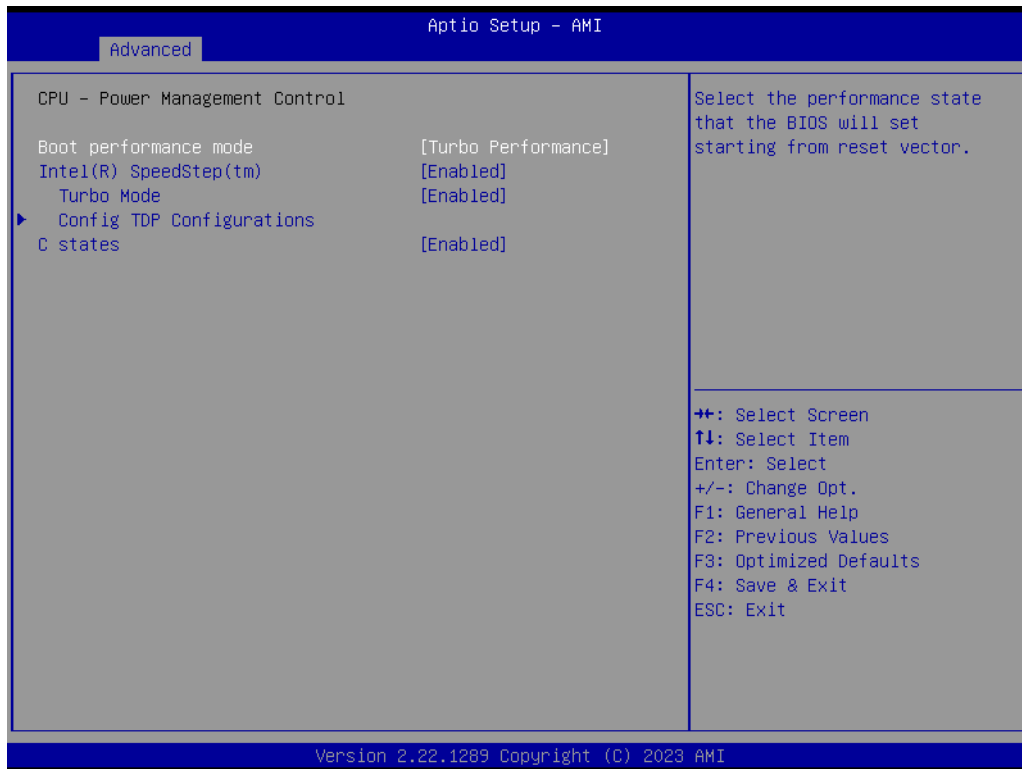
## 3.4.2 Power & Performance



**Figure 3.5 Power & Performance**

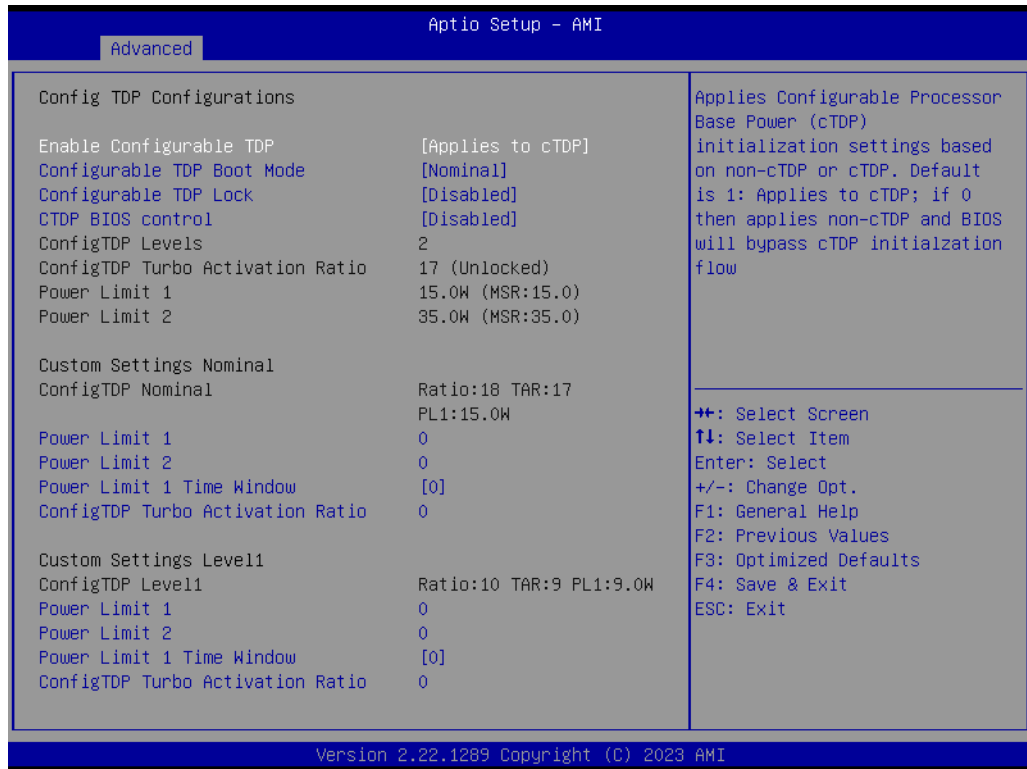
- **CPU - Power Management Control**  
CPU - Power Management Control Options.
- **GT - Power Management Control**  
GT - Power Management Control Options.

### 3.4.2.1 CPU - Power Management Control



**Figure 3.6 CPU - Power Management Control**

- **Boot performance mode**  
Select the performance state that the BIOS will set starting from the reset vector.
- **Intel(R) SpeedStep(tm)**  
Allows more than two frequency ranges to be supported.
- **Turbo Mode**  
Enable/Disable processor Turbo Mode (requires EMTTM enabled too). AUTO means enabled.
- **Config TDP Configurations**  
Configurable Processor Base Power (cTDP) Configurations.
- **C states**  
Enable/Disable CPU Power Management. Allows CPU to go to C states when it is not 100% utilized.

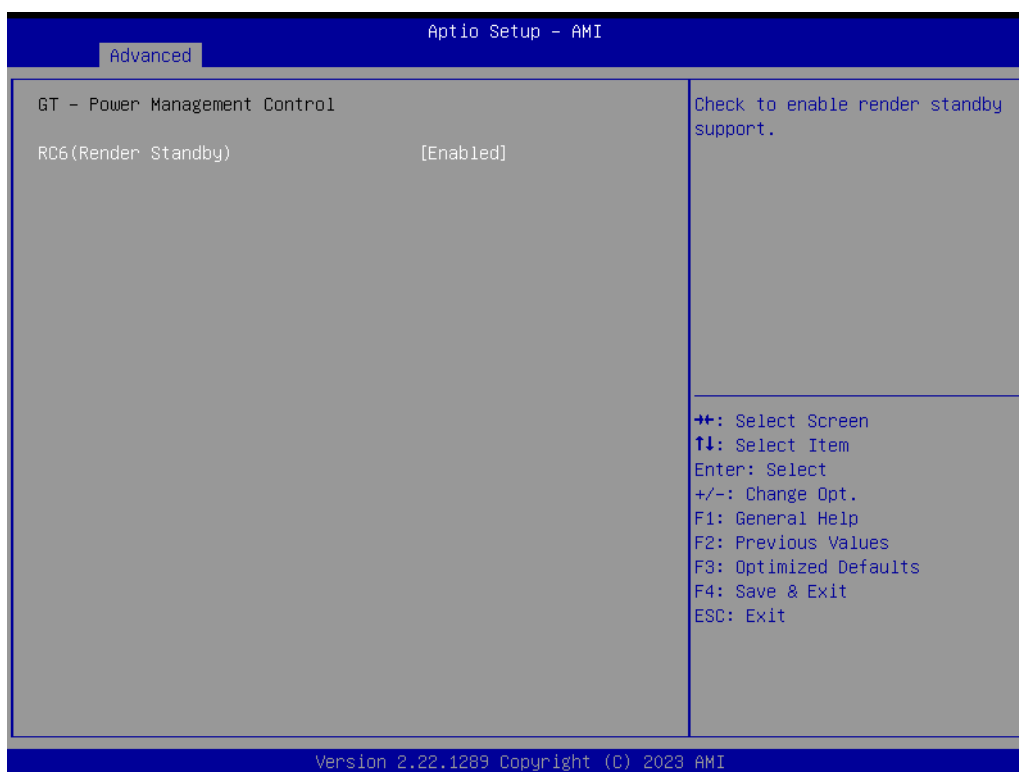


**Figure 3.7 Config TDP Configurations**

- **Enable Configurable TDP**  
 Applies Configurable Processor Base Power (cTDP) initialization settings based on non-cTDP or cTDP. Default is 1: Applies to cTDP? if 0 then applies non-cTDP? If 0 then applies non-cTDP and BIOS will bypass cTDP initialization flow.
- **Configurable TDP Boot Mode**  
 Configurable Processor Base Power (cTDP) Mode as Nominal/Level1/Level2/ Deactivate TDP selection. Deactivate option will set MSR to Nominal and MMIO to Zero.
- **Configurable TDP Lock**  
 Configurable Processor Base Power (cTDP) Mode Lock sets the Lock bits on TURBO\_ACTIVATION\_RATIO and CONFIG\_TDP\_CONTROL. Note: When CTDP Lock is enabled, Custom ConfigTDP Count will be forced to 1 and Custom ConfigTDP Boot Index will be forced to 0.
- **CTDP BIOS control**  
 Enable Configurable Processor Base Power (cTDP) control via runtime ACPI BIOS methods. This “BIOS only” feature does not require EC or driver support.
- **Power Limit 1**  
 Power Limit1 in milliwatts. BIOS will round to the nearest 1/8W when programming. 0=no custom override. For 12.50W, enter 12500. Overlocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE\_POWER\_SKU\_MSR). Other SKUs: This value must be between Min Power Limit and Processor Base Power (TDP) Limit.
- **Power Limit 2**  
 Power Limit2 in milliwatts. BIOS will round to the nearest 1/8W when programming. 0=no custom override. For 12.50W, enter 12500. The processor applies control policies such that the package power does not exceed this limit.

- **Power Limit 1 Time Window**  
Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0=default value (28 sec for Mobile and 8 sec for Desktop). It defines the time window in which the Processor Base Power (TDP) value should be maintained.
- **ConfigTDP Turbo activation Ratio**  
Custom value for Turbo Activation Ratio. It needs to be configured with valid values from LFM to Max Turbo. 0 means it does not use a custom value.
- **Power Limit 1**  
Power Limit1 in milliwatts. BIOS will round to the nearest 1/8W when programming. 0=no custom override. For 12.50W, enter 12500. Overclocking SKU: Value must be between Max and Min Power Limits (specified by PACKAGE\_POWER\_SKU\_MSR). Other SKUs: This value must be between the Min Power Limit and Processor Base Power (TDP) Limit.
- **Power Limit 2**  
Power Limit2 in milliwatts. BIOS will round to the nearest 1/8W when programming. 0=no custom override. For 12.50W, enter 12500. The processor applies control policies such that the package power does not exceed this limit.
- **Power Limit 1 Time Window**  
Power Limit 1 Time Window value in seconds. The value may vary from 0 to 128. 0=default value (28sec for Mobile and 8 sec for Desktop). It defines the time window in which the Processor Base Power (TDP) value should be maintained.
- **ConfigTDP Turbo activation Ratio**  
Custom value for the Turbo Activation Ratio. It needs to be configured with valid values from LFM to Max Turbo. 0 means it does not use a custom value.

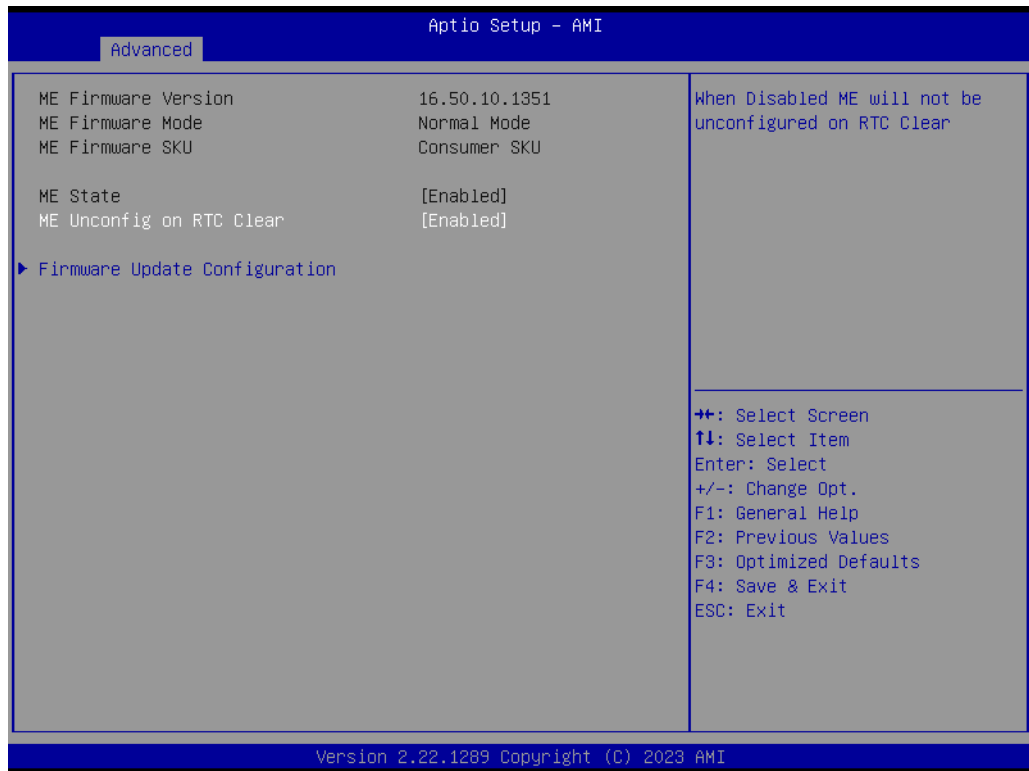
### 3.4.2.2 GT - Power Management Control



**Figure 3.8 GT - Power Management Control**

- **RC6 (Render Standby)**  
Check to enable render standby support.

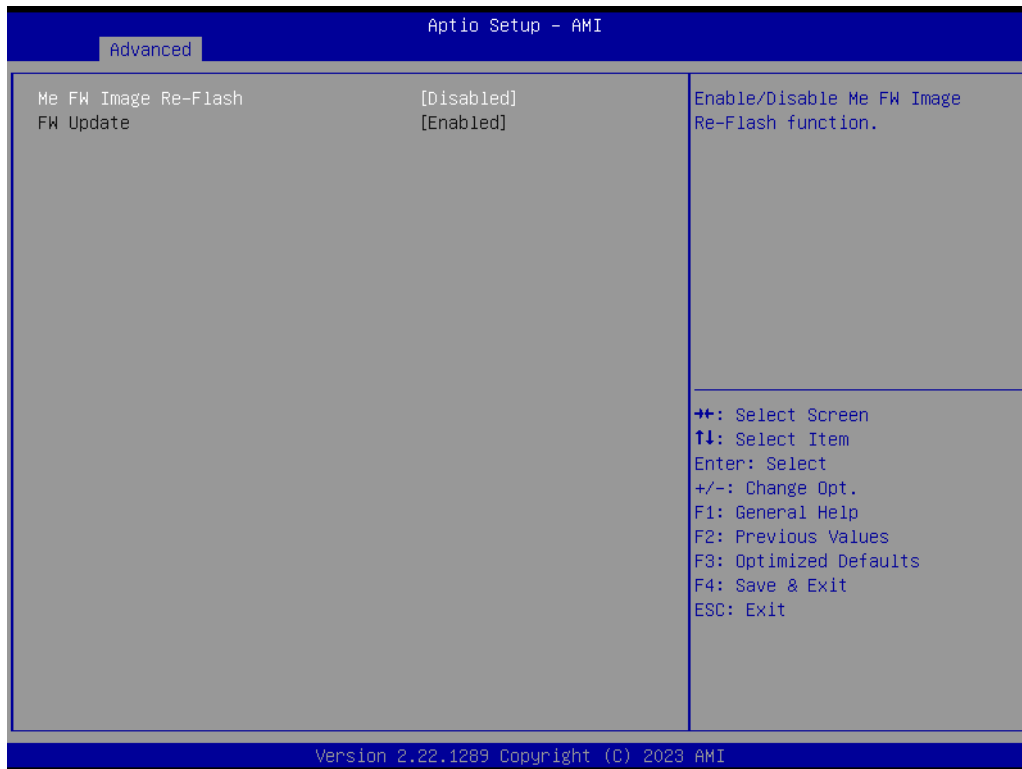
### 3.4.3 PCH-FW Configuration



**Figure 3.9 PCH-FW Configuration**

- **ME State**  
When Disabled, ME will be put into ME Temporarily Disabled Mode.
- **ME Unconfig on RTC Clear**  
When Disabled, ME will not be unconfigured on RTC clear.
- **Firmware Update Configuration**  
Configure Management Engine Technology Parameters.

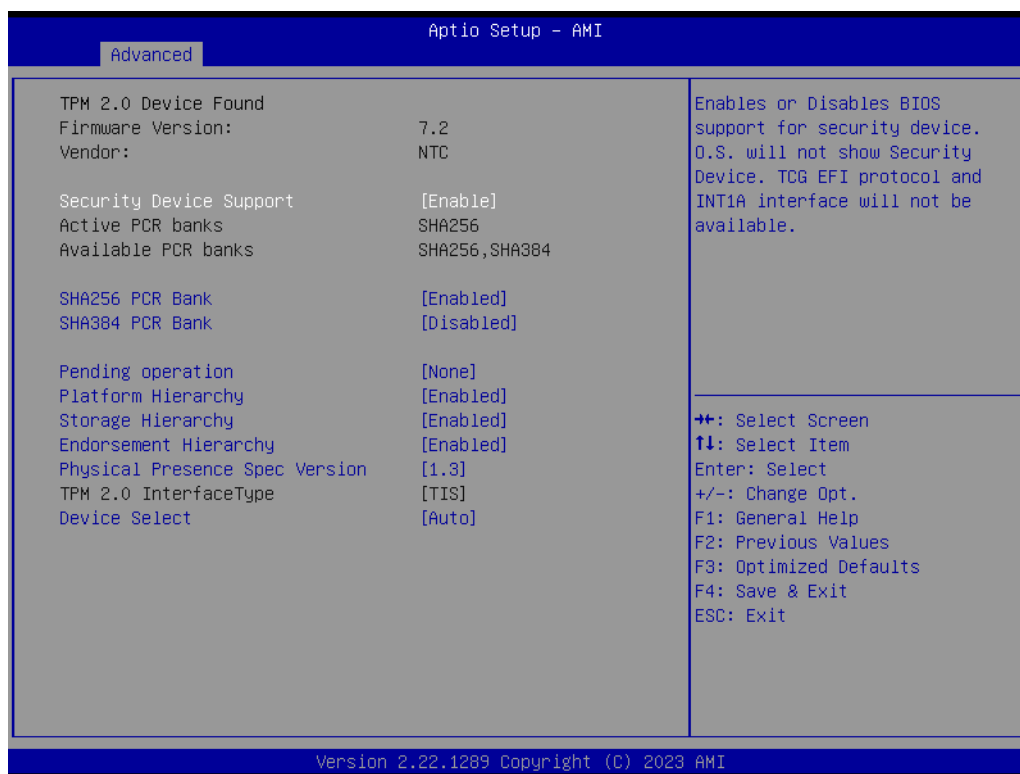
### 3.4.3.1 Firmware Update Configuration



**Figure 3.10 Firmware Update Configuration**

- **Me FW Image Re-Flash**  
Enable/Disable the Me FW Image Re-Flash function.
- **FW Update**  
Enable/Disable the ME FW Update function.

## 3.4.4 Trusted Computing

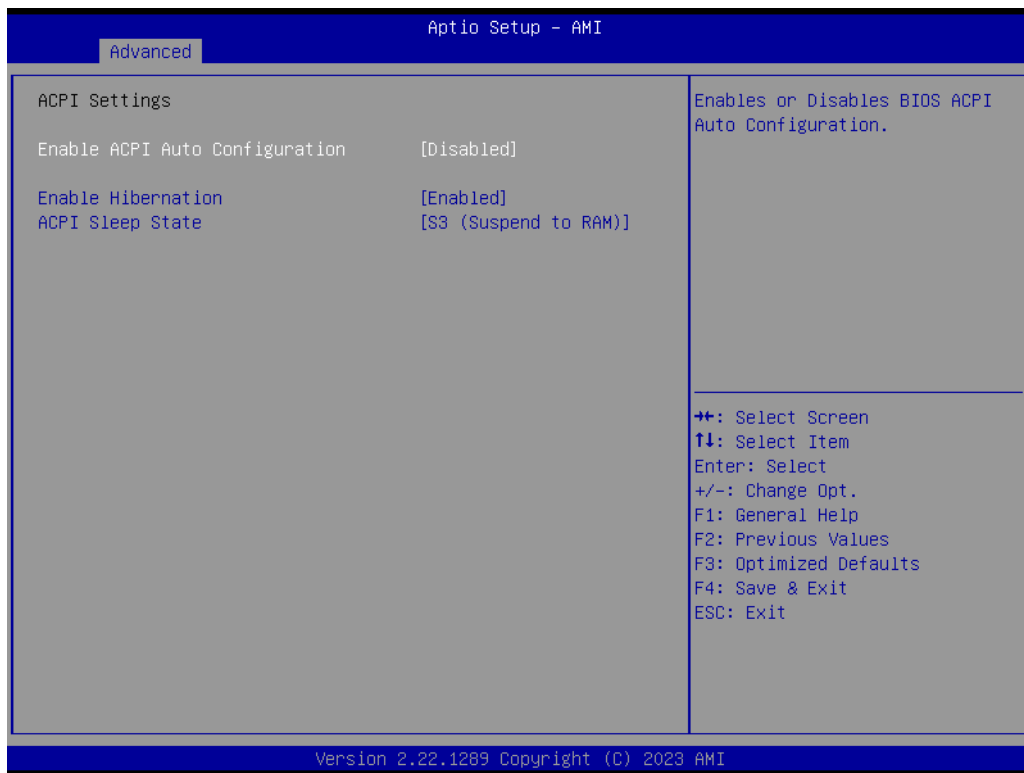


**Figure 3.11 Trusted Computing**

- **Security Device Support**  
Enable or Disable BIOS support for a security device. The OS will not show the Security Device. TCG EFI protocol and INT1A interfaces will not be available.
- **SHA256 PCR Bank**  
Enable or Disable SHA256 PCR Bank.
- **SHA384 PCR Bank**  
Enable or Disable SHA384 PCR Bank.
- **Pending operation**  
Schedule an operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change the State of Security Device.
- **Platform Hierarchy**  
Enable or Disable Platform Hierarchy.
- **Storage Hierarchy**  
Enable or Disable Storage Hierarchy.
- **Endorsement Hierarchy**  
Enable or Disable Endorsement Hierarchy.
- **Physical Presence Spec Version**  
Select to tell the OS to support PPI Spec Version 1.2 or 1.3. Note: some HCK tests might not support 1.3.
- **Device Select**  
TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices. Auto will support both with the default set to TPM 2.0 devices if not found. TPM 1.2 devices will be enumerated.



### 3.4.5 ACPI Settings



**Figure 3.12 ACPI Settings**

- **Enable ACPI Auto Configuration**  
Enable or Disable BIOS ACPI Auto Configuration.
- **Enable Hibernation**  
Enable or Disable the System's ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
- **ACPI Sleep State**  
Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.

## 3.4.6 Embedded Controller

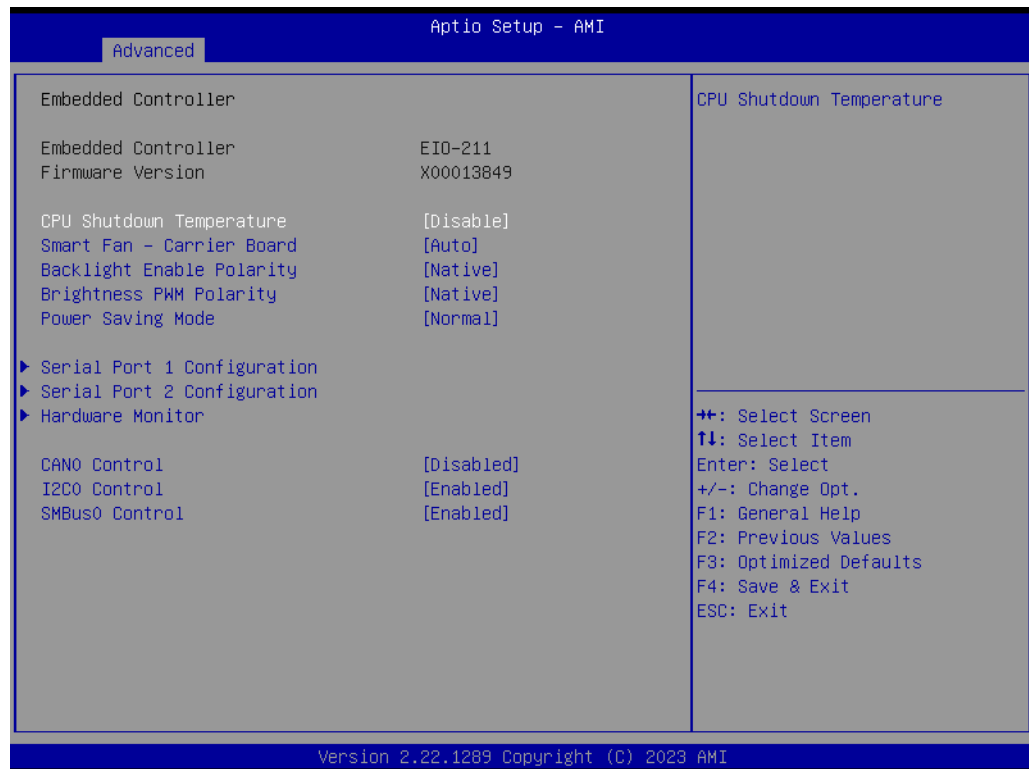
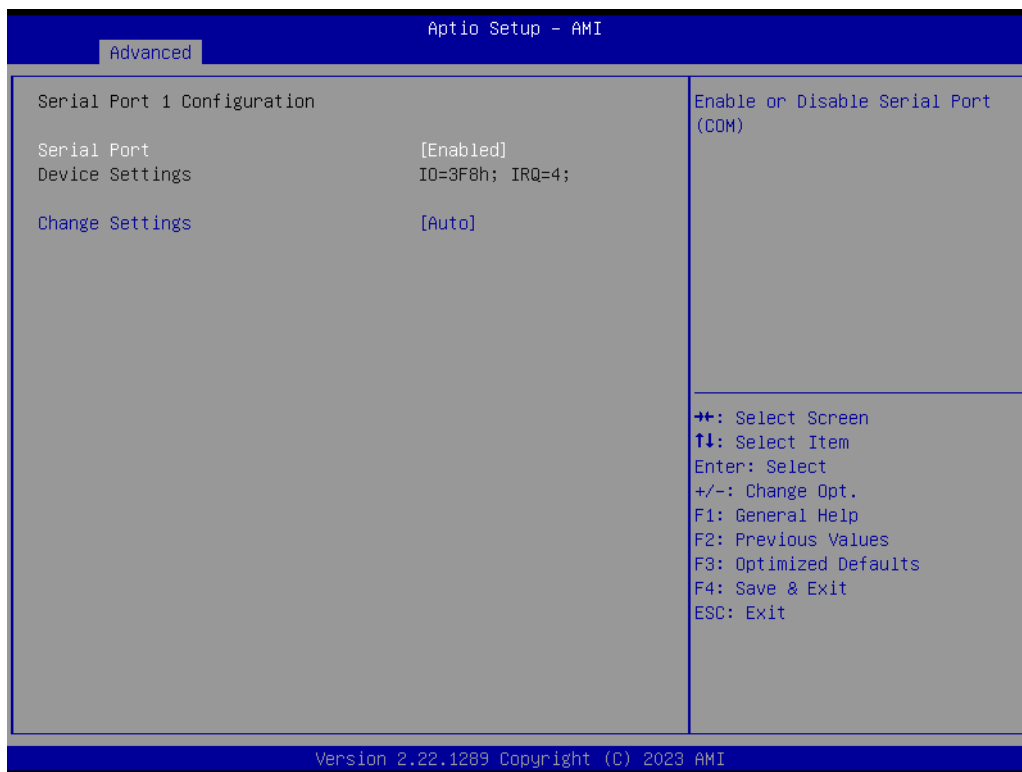


Figure 3.13 Embedded Controller

- **CPU Shutdown Temperature**  
CPU Shutdown Temperature.
- **Smart Fan - Carrier Board**  
Control Carrier Board Smart FAN function. It gets the value from EC and only sets the value when Saving Changes.
- **Backlight Enable Polarity**  
Switch Backlight Enable Polarity to Native or Invert.
- **Brightness PWM Polarity**  
Backlight Control Brightness PWM Polarity for Native or Invert.
- **Power Saving Mode**  
Select Power Saving Mode.
- **Serial Port 1 Configuration**  
Set Parameters of Serial Port 1 (COMA).
- **Serial Port 2 Configuration**  
Set Parameters of Serial Port 2 (COMB).
- **Hardware Monitor**  
Monitor hardware status.
- **CAN0 Control**  
Enable/Disable CAN0 controller on RDC-IS200.
- **I2C0 Control**  
Enable/Disable I2C0 controller on RDC-IS200.
- **SMBus0 Control**  
Enable/Disable SMBus0 controller on RDC-IS200.

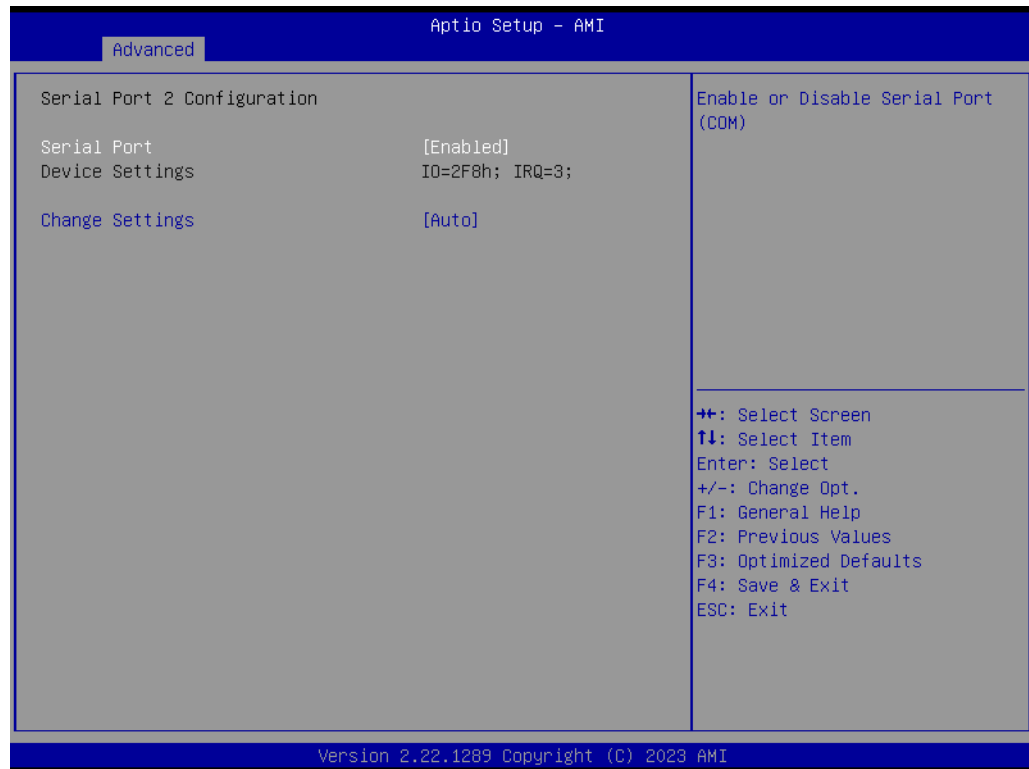
### 3.4.6.1 Serial Port 1 Configuration



**Figure 3.14 Serial Port 1 Configuration**

- **Serial Port**  
Enable or Disable Serial Port (COM).
- **Change Settings**  
Select an optimal setting for a Super IO Device.

### 3.4.6.2 Serial Port 2 Configuration



**Figure 3.15 Serial Port 2 Configuration**

- **Serial Port**  
Enable or Disable Serial Port (COM).
- **Change Settings**  
Select optimal settings for a Super IO Device.

### 3.4.6.3 Hardware Monitor

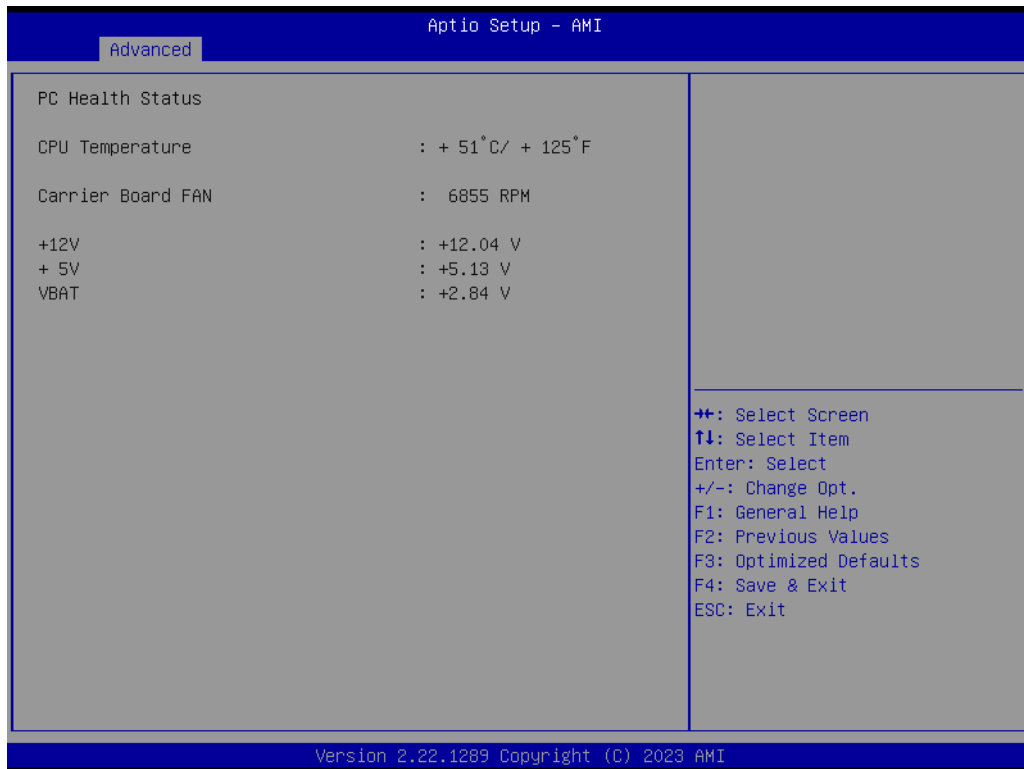


Figure 3.16 Hardware Monitor

## 3.4.7 Serial Port Console Redirection

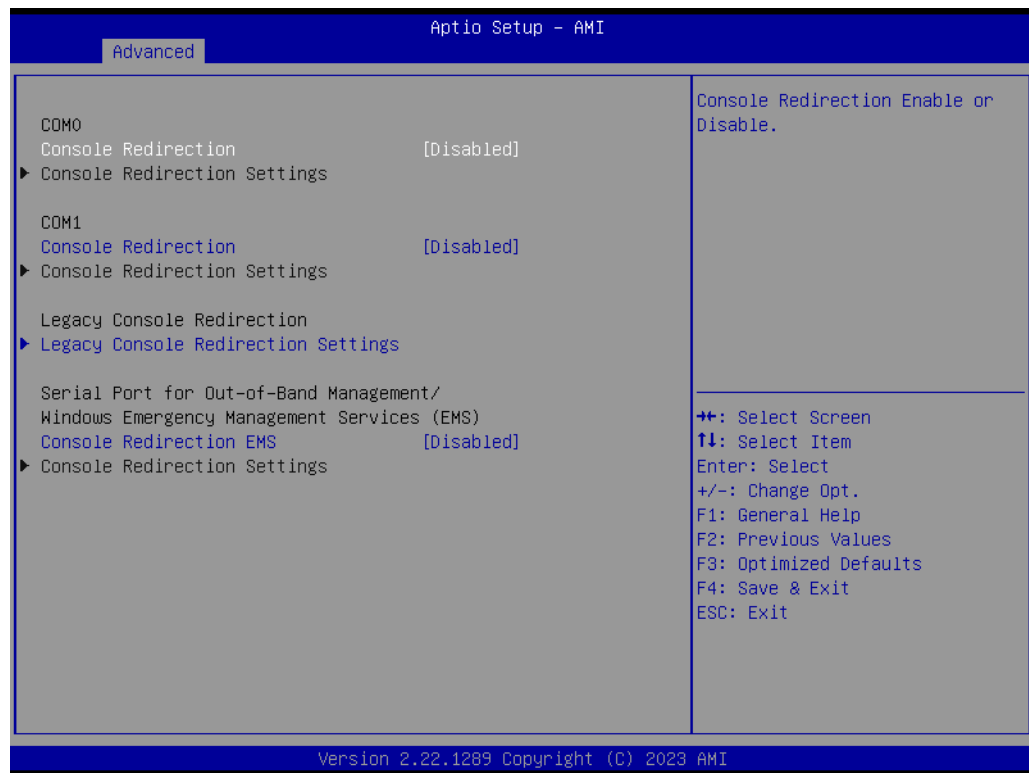
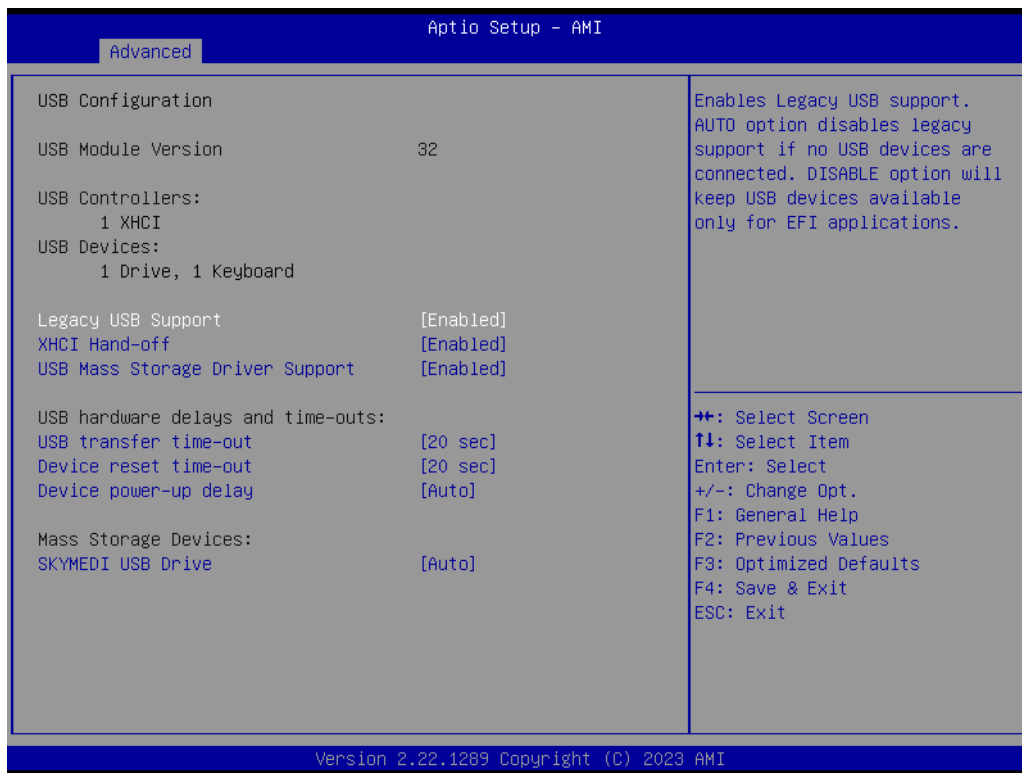


Figure 3.17 Serial Port console Redirection

- **COM1 Console Redirection**  
Console Redirection Enable or Disable.
- **Legacy Console Redirection Settings**  
Legacy Console Redirection Settings.
- **Console Redirection EMS**  
Console Redirection Enable or Disable.

### 3.4.8 USB Configuration



**Figure 3.18 USB Configuration**

- **Legacy USB Support**  
Enable Legacy USB support. The AUTO option disables legacy support if no USB devices are connected. The DISABLE option will keep USB devices available only for EFI applications.
- **XHCI Hand-off**  
This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI driver.
- **USB Mass Storage Driver Support**  
Enable/Disable USB Mass Storage Driver Support.
- **USB transfer time-out**  
The time-out value for Control, Bulk, and Interrupt transfers.
- **Device reset time-out**  
USB mass storage device Start Unit command time-out.
- **Device power-up delay**  
Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses the default value: for a Root port it is 100 ms, for a Hub port the delay is taken from the Hub descriptor.

## 3.4.9 OEM Configuration

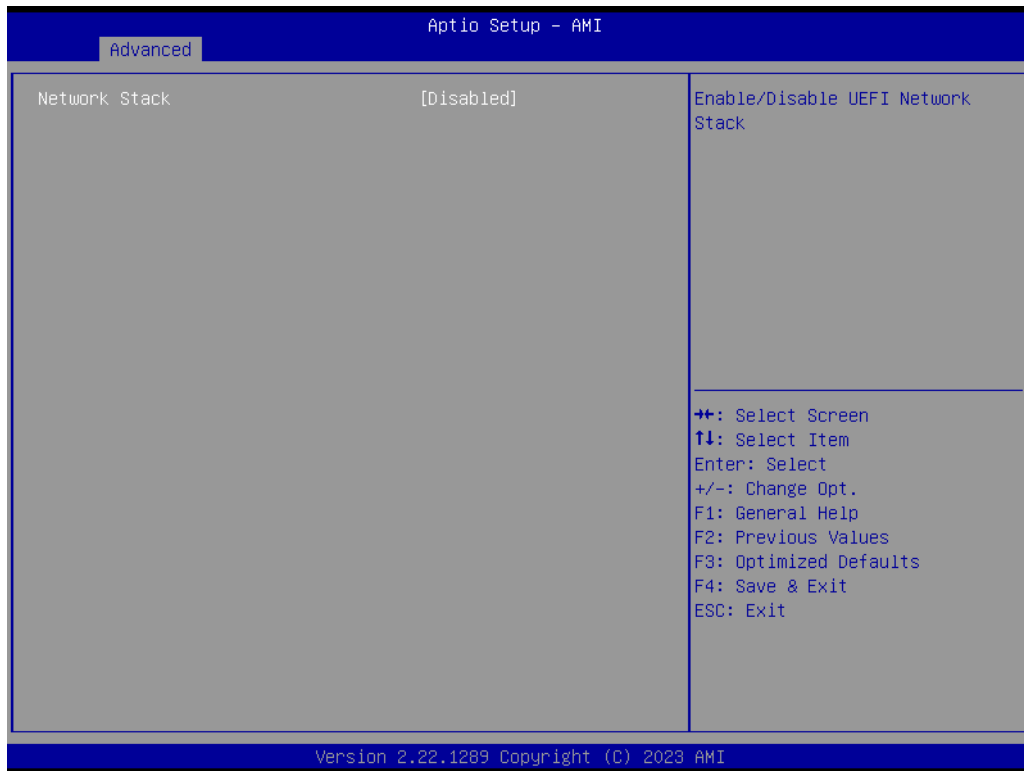


**Figure 3.19 OEM Configuration**

- **SATA\_LED/SPKR Pin Control**  
Select GPP\_B14 pin function to Serial ATA LED or Speaker Output. Hybrid: SPKR in pre-boot, SATA LED in runtime.



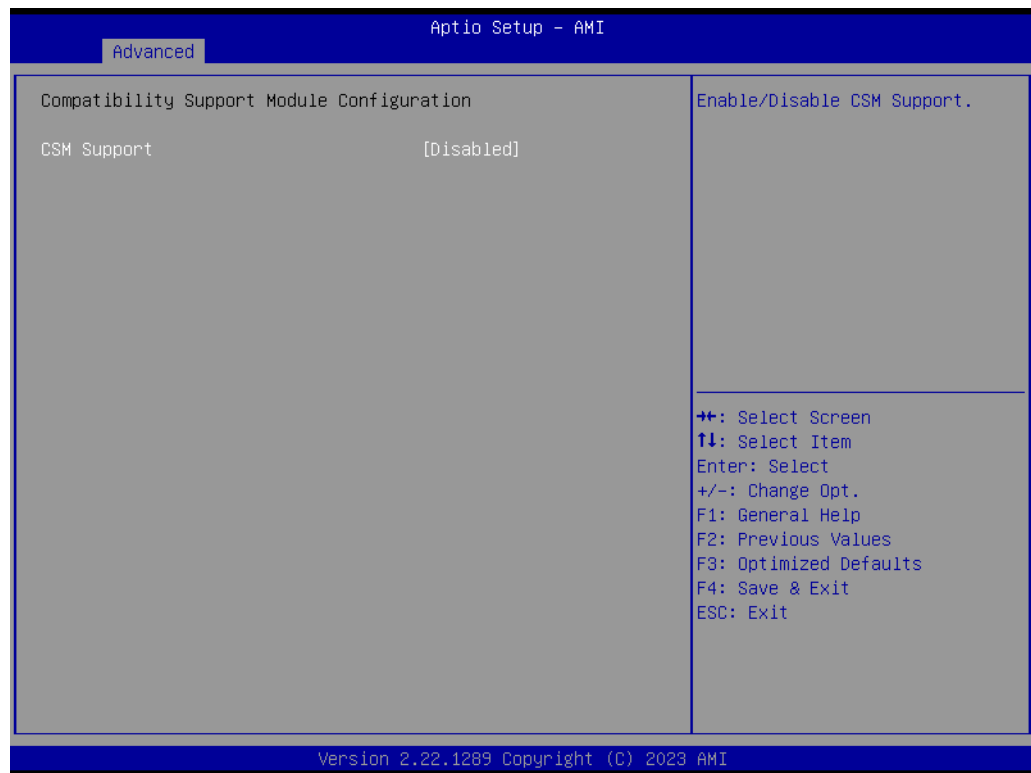
### 3.4.10 Network Stack Configuration



**Figure 3.20 Network Stack Configuration**

- **Network Stack**  
Enable/Disable UEFI Network Stack.

### 3.4.11 Compatibility Support Module Configuration



**Figure 3.21 Compatibility Support Module Configuration**

- **CSM Support**  
Enable/Disable CSM Support.

## 3.5 Chipset Setup

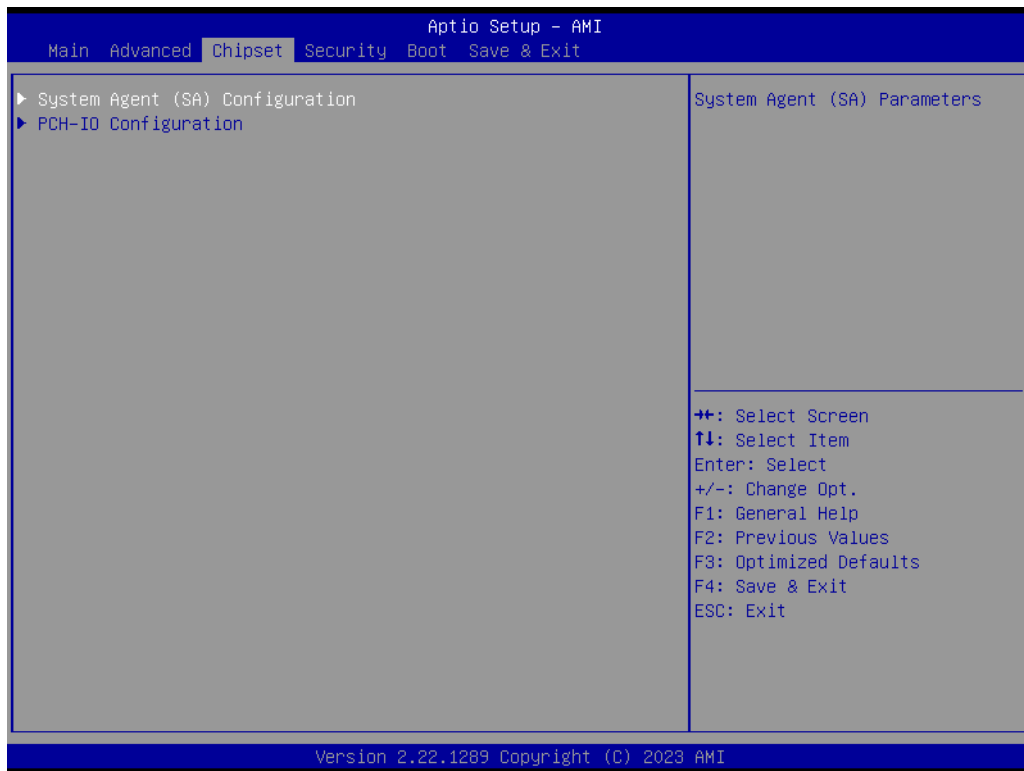
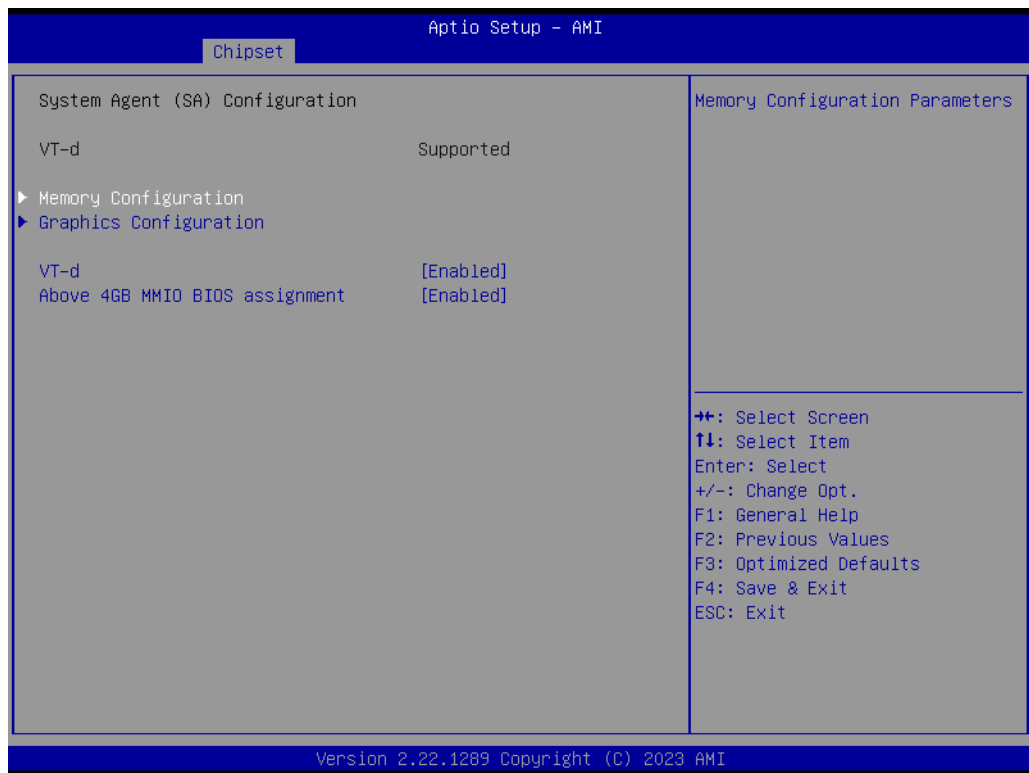


Figure 3.22 Chipset Setup

- **System Agent (SA) Configuration**  
System Agent Parameters.
- **PCH-I/O Configuration**  
PCH parameters.

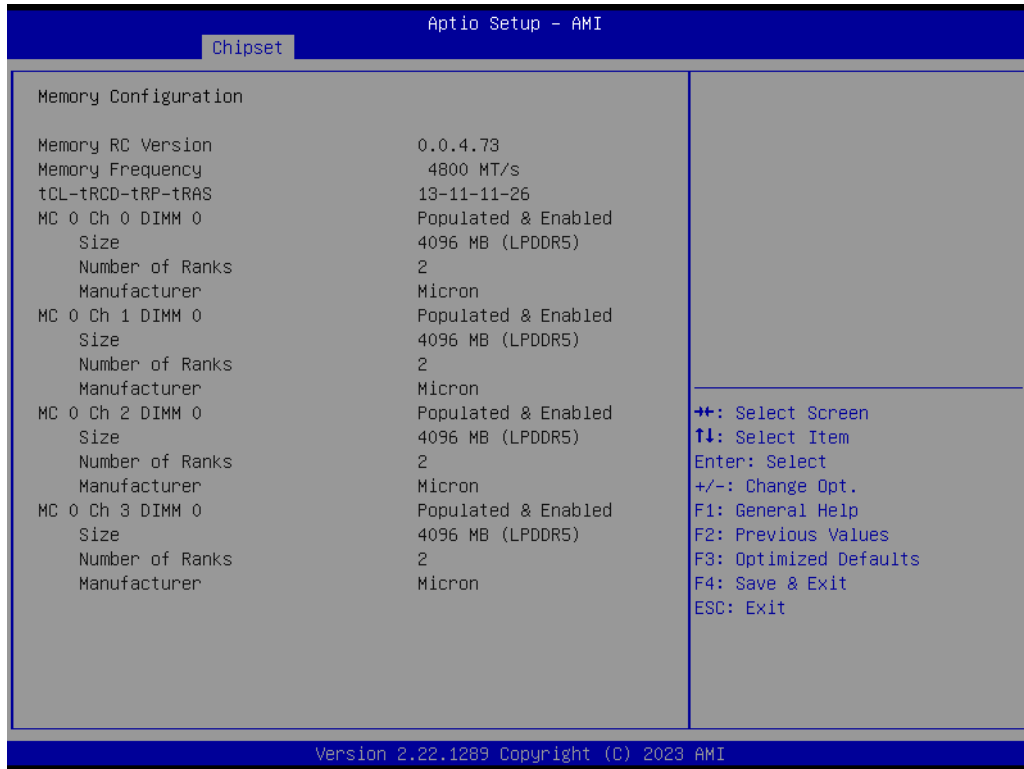
## 3.5.1 System Agent (SA) Configuration



**Figure 3.23 System Agent (SA) Configuration**

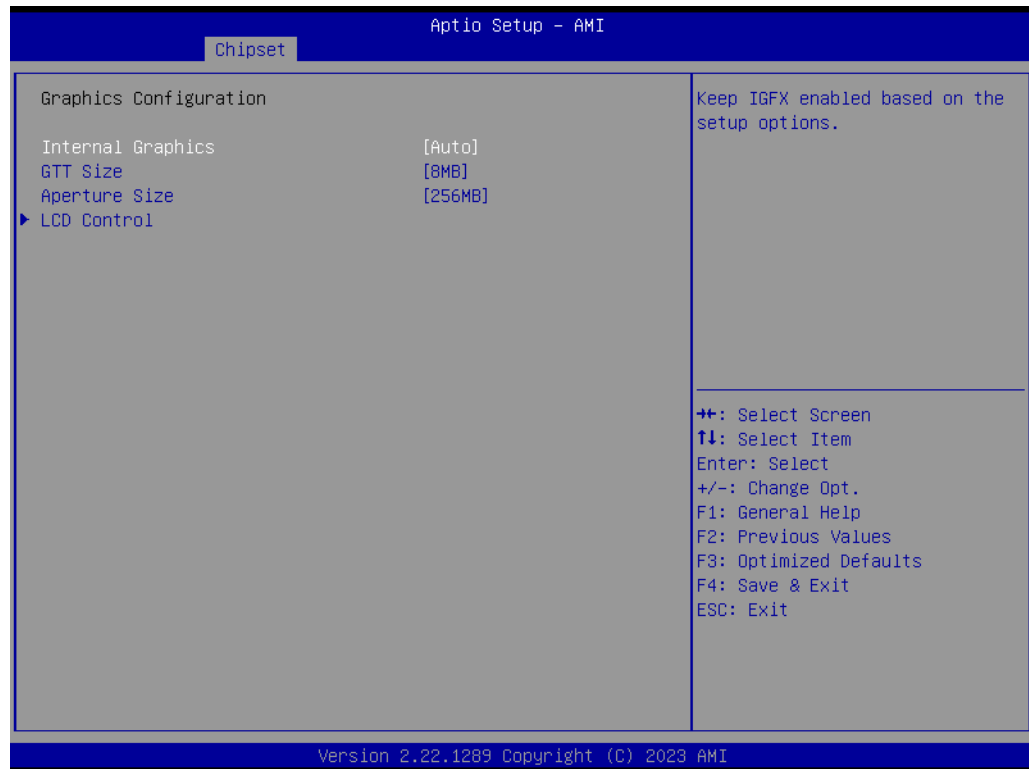
- **Memory Configuration**  
Memory Configuration Parameters.
- **Graphics Configuration**  
Graphics Configuration.
- **VT-d**  
VT-d capability.
- **Above 4GB MMIO BIOS assignment**  
Enable/Disable above 4GB memory mapped IO BIOS assignment. This is enabled automatically when aperture size is set to 2048MB.

### 3.5.1.1 Memory Configuration



**Figure 3.24 Memory Configuration**

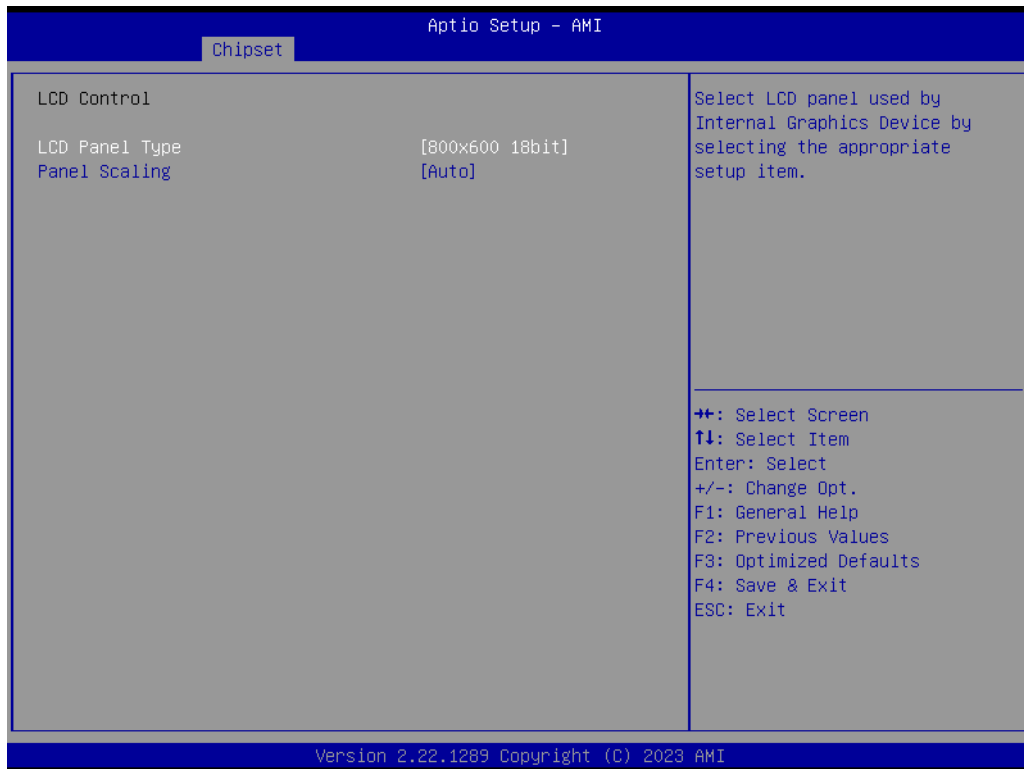
### 3.5.1.2 Graphics Configuration



**Figure 3.25 Graphics Configuration**

- **Internal Graphics**  
Keep IGFX enabled based on the setup options.
- **GTT Size**  
Select the GTT size.
- **Aperture Size**  
Select the aperture size. Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM support.
- **LCD Control**  
LCD Control.

## ■ LCD Control



**Figure 3.26 LCD Control**

- **LCD Panel Type**  
Select the LCD panel used by the Internal Graphics Device by selecting the appropriate setup item.
- **Panel Scaling**  
Select the LCD panel scaling option used by the Internal Graphics Device.

## 3.5.2 PCH-IO Configuration

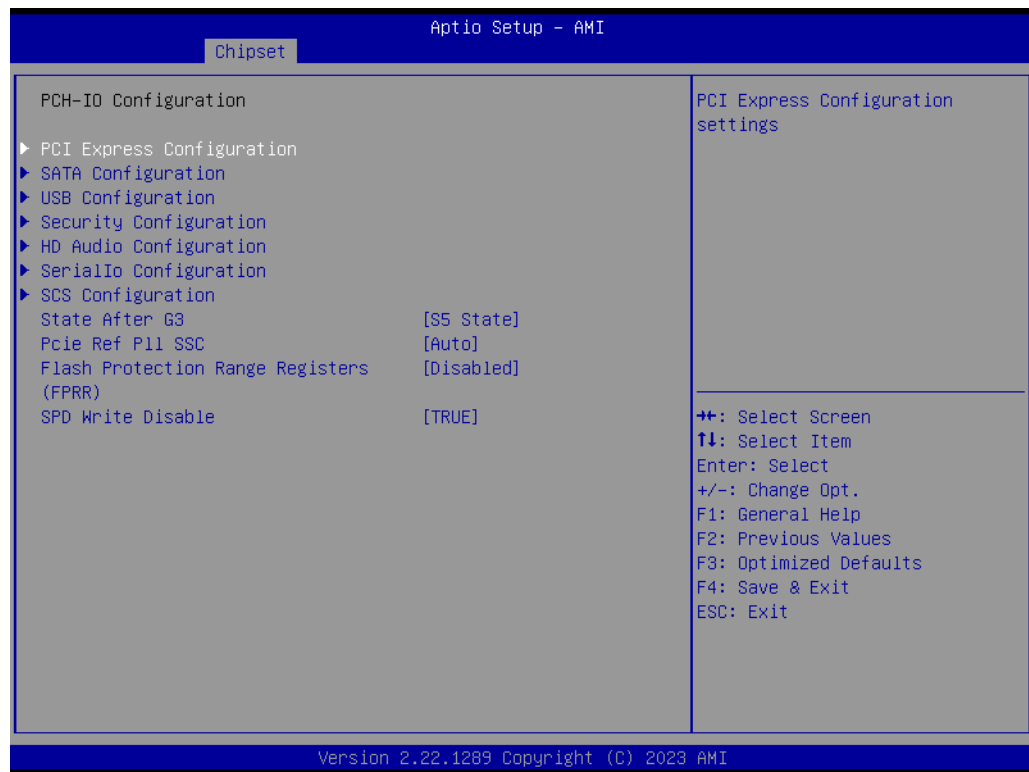
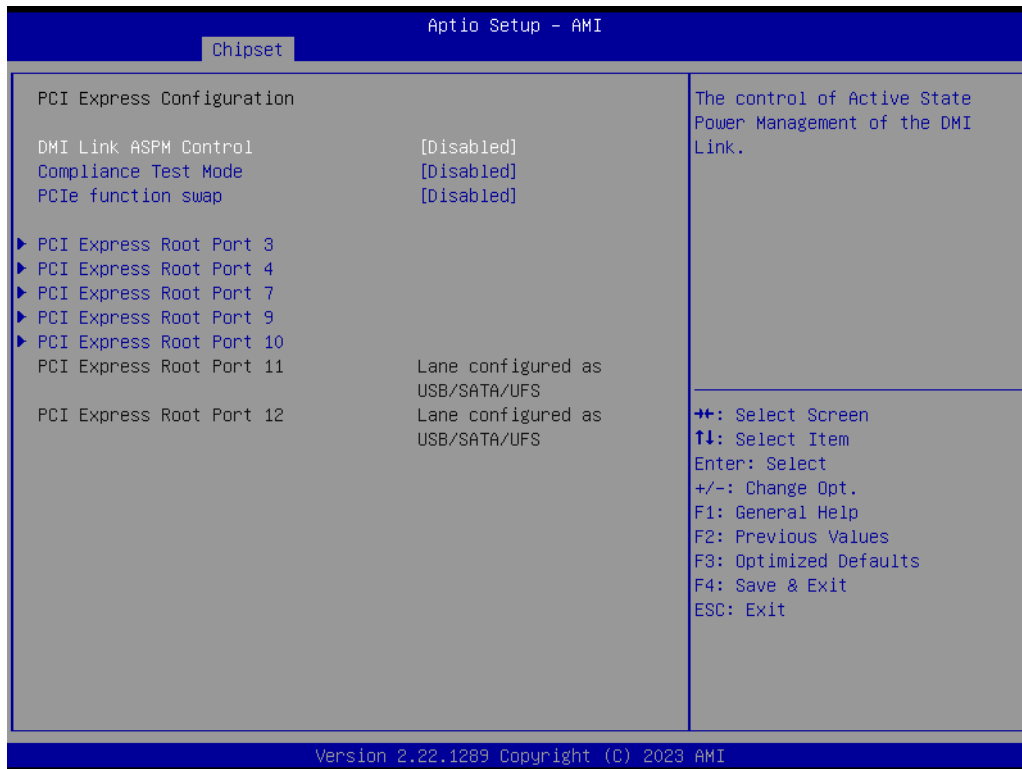


Figure 3.27 PCH-IO Configuration

- **PCI Express Configuration**  
PCI Express Configuration settings.
- **SATA Configuration**  
SATA device option settings.
- **USB Configuration**  
USB Configuration settings.
- **Security Configuration**  
Security Configuration settings.
- **HD Audio Configuration**  
HD audio subsystem configuration settings.
- **SerialIo Configuration**  
SerialIo configuration settings.
- **SCS Configuration**  
Storage and Communication Subsystem (SCS) Configuration.



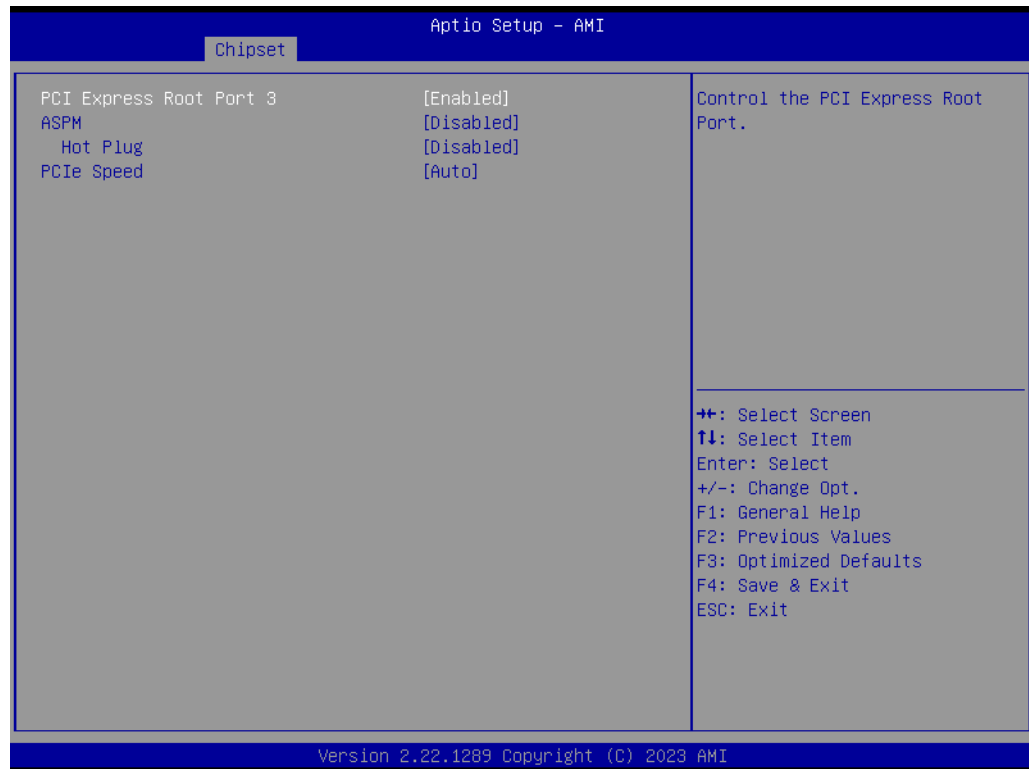
### 3.5.2.1 PCI Express Configuration



**Figure 3.28 PCI Express Configuration**

- **DMI Link ASPM Control**  
The control of Active State Power Management of the DMI Link.
- **Compliance Test Mode**  
Enable when using Compliance Load Board.
- **PCIe function swap**  
When Disabled, it prevents PCIE rootport function swap. If any function other than 0th is enabled, 0th will become visible.
- **PCI Express Root Port 3**  
PCI Express Root Port Settings.
- **PCI Express Root Port 4**  
PCI Express Root Port Settings.
- **PCI Express Root Port 7**  
PCI Express Root Port Settings.
- **PCI Express Root Port 9**  
PCI Express Root Port Settings.
- **PCI Express Root Port 10**  
PCI Express Root Port Settings.

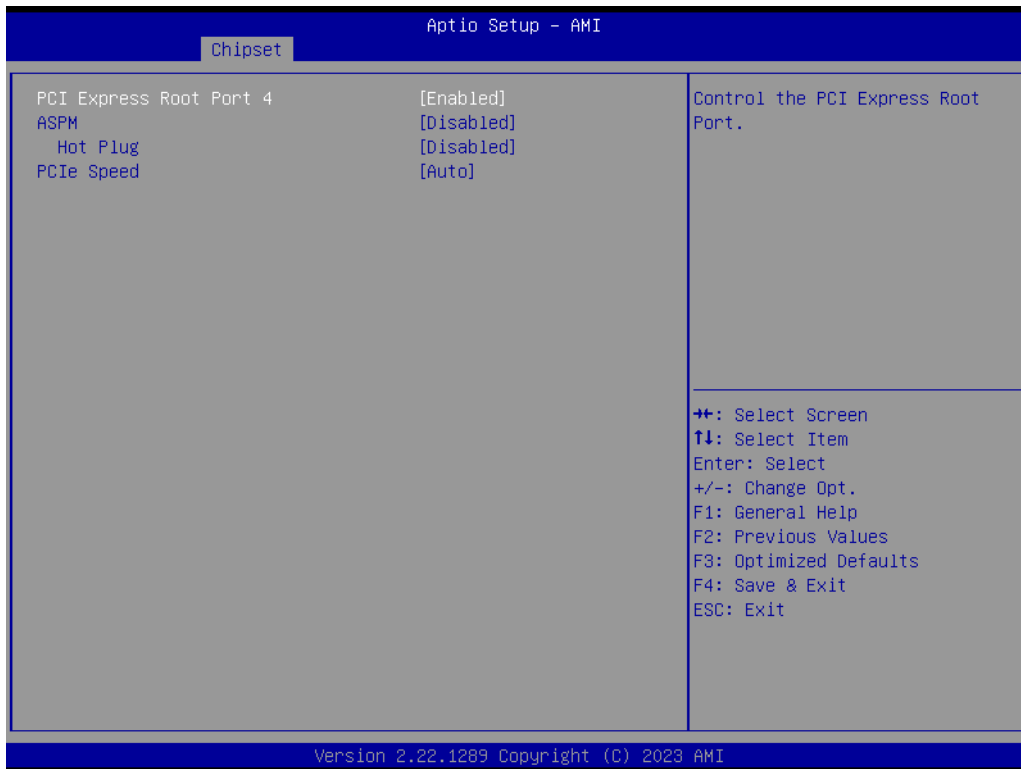
## ■ PCI Express Root Port 3



**Figure 3.29 PCI Express Root Port 3**

- **PCI Express Root Port 3**  
Control the PCI Express Root Port.
- **ASPM**  
Set the ASPM Level: Force L0s – Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disables ASPM.
- **Hot Plug**  
PCI Express Hot Plug Enable/Disable.
- **PCIe Speed**  
Configure PCIe Speed.

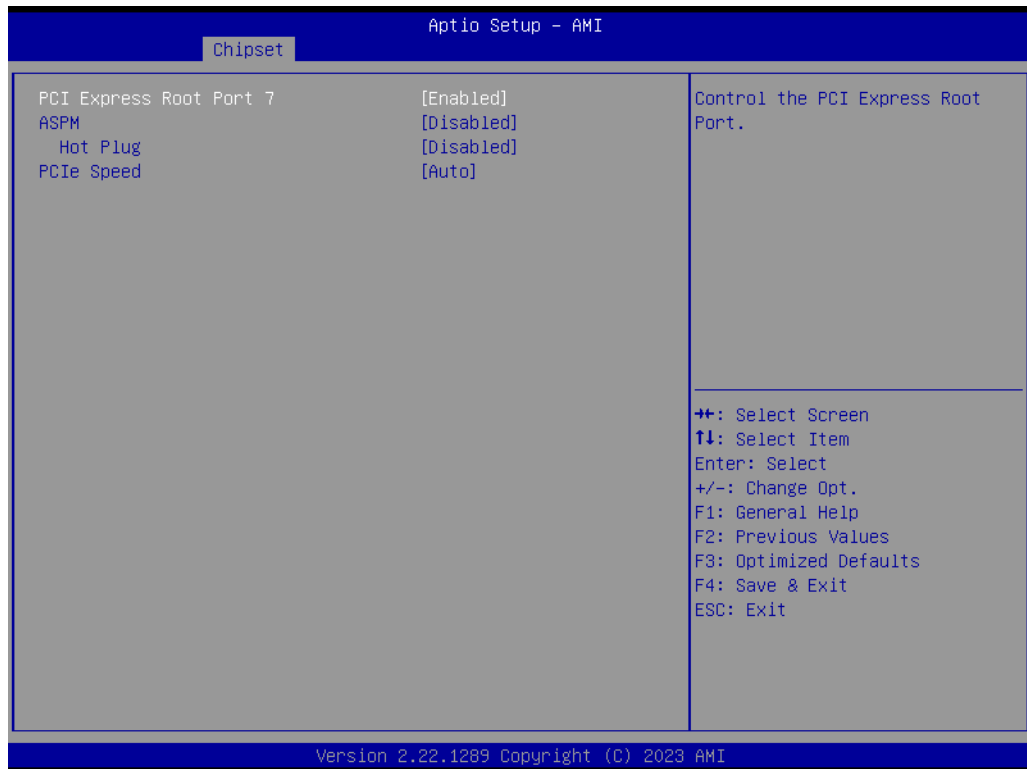
## ■ PCI Express Root Port 4



**Figure 3.30 PCI Express Root Port 4**

- **PCI Express Root Port 4**  
Control the PCI Express Root Port.
- **ASPM**  
Set the ASPM Level: Force L0s – Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disables ASPM.
- **Hot Plug**  
PCI Express Hot Plug Enable/Disable.
- **PCIe Speed**  
Configure PCIe Speed.

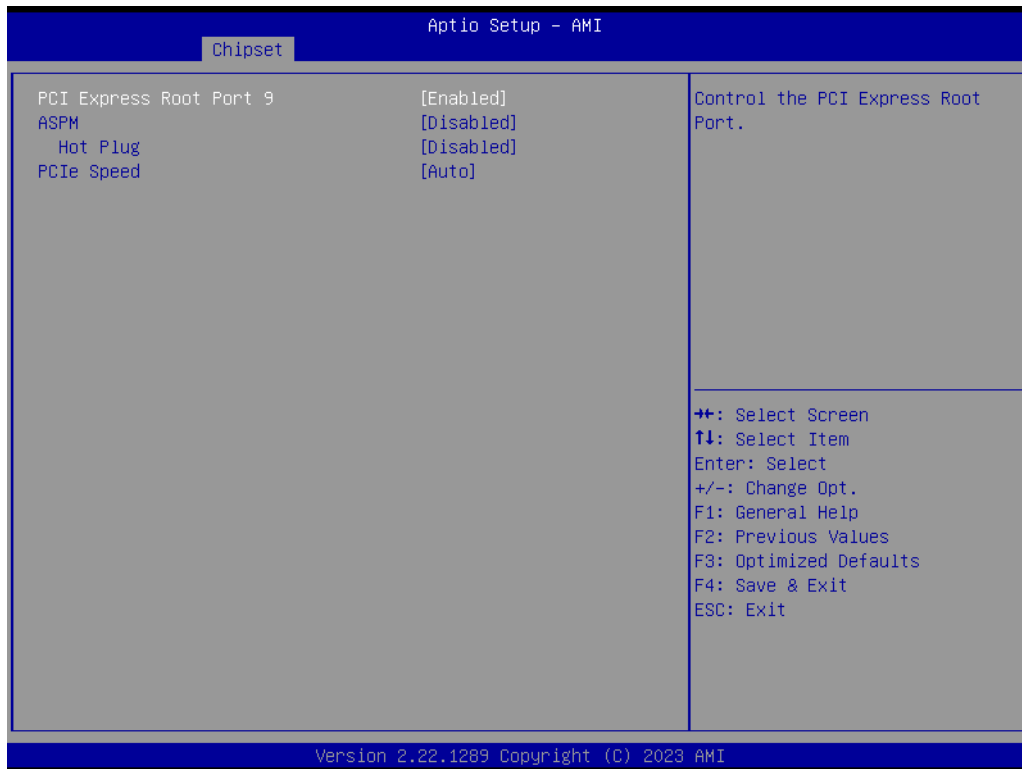
## ■ PCI Express Root Port 7



**Figure 3.31 PCI Express Root Port 7**

- **PCI Express Root Port 7**  
Control the PCI Express Root Port.
- **ASPM**  
Set the ASPM Level: Force L0s – Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disables ASPM.
- **Hot Plug**  
PCI Express Hot Plug Enable/Disable.
- **PCIe Speed**  
Configure PCIe Speed.

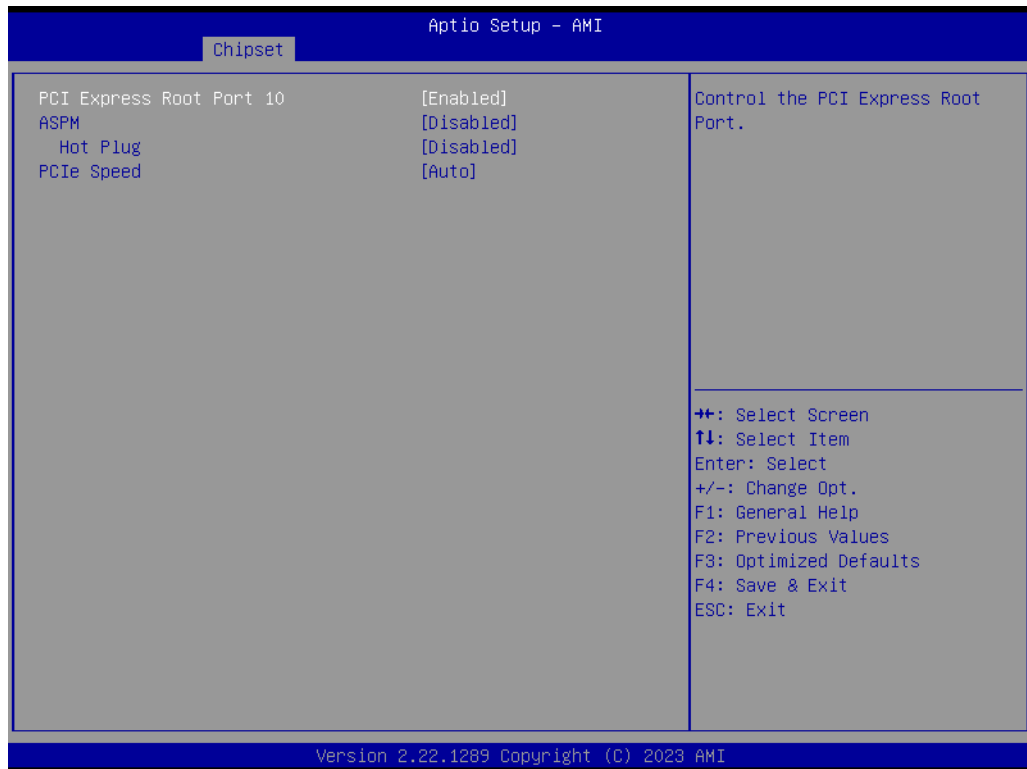
## ■ PCI Express Root Port 9



**Figure 3.32 PCI Express Root Port 9**

- **PCI Express Root Port 9**  
Control the PCI Express Root Port.
- **ASPM**  
Set the ASPM Level: Force L0s – Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disables ASPM.
- **Hot Plug**  
PCI Express Hot Plug Enable/Disable.
- **PCIe Speed**  
Configure PCIe Speed.

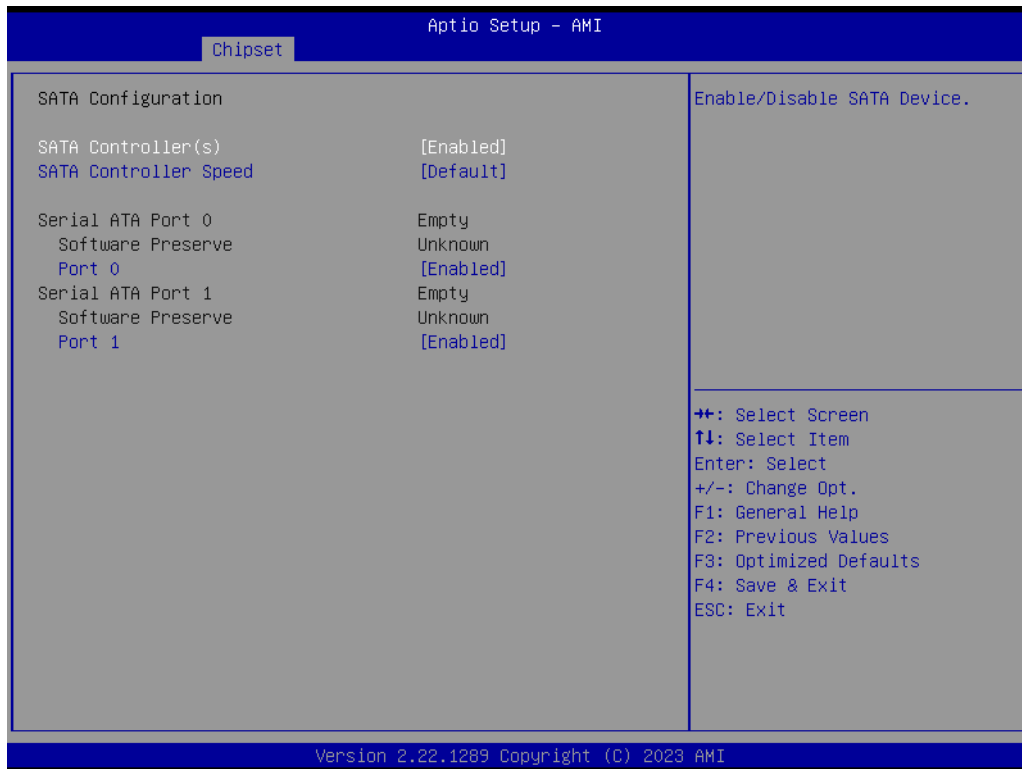
## ■ PCI Express Root Port 10



**Figure 3.33 PCI Express Root Port 10**

- **PCI Express Root Port 10**  
Control the PCI Express Root Port.
- **ASPM**  
Set the ASPM Level: Force L0s – Force all links to L0s State AUTO – BIOS auto configure DISABLE – Disables ASPM.
- **Hot Plug**  
PCI Express Hot Plug Enable/Disable.
- **PCIe Speed**  
Configure PCIe Speed.

### 3.5.2.2 SATA Configuration



**Figure 3.34 SATA Configuration**

- **SATA Controller(s)**  
Enable/Disable an SATA Device.
- **SATA Controller Speed**  
Indicates the maximum speed the SATA controller can support.
- **Port 0**  
Enable or Disable the SATA Port.
- **Port 1**  
Enable or Disable the SATA Port.

### 3.5.2.3 USB Configuration

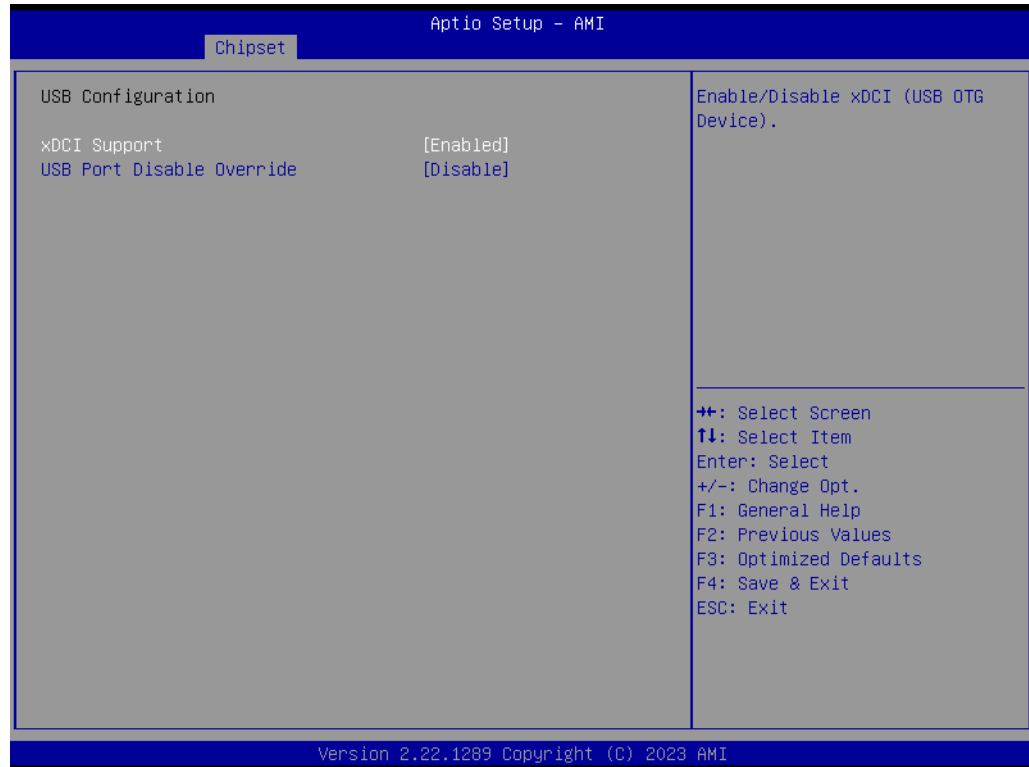
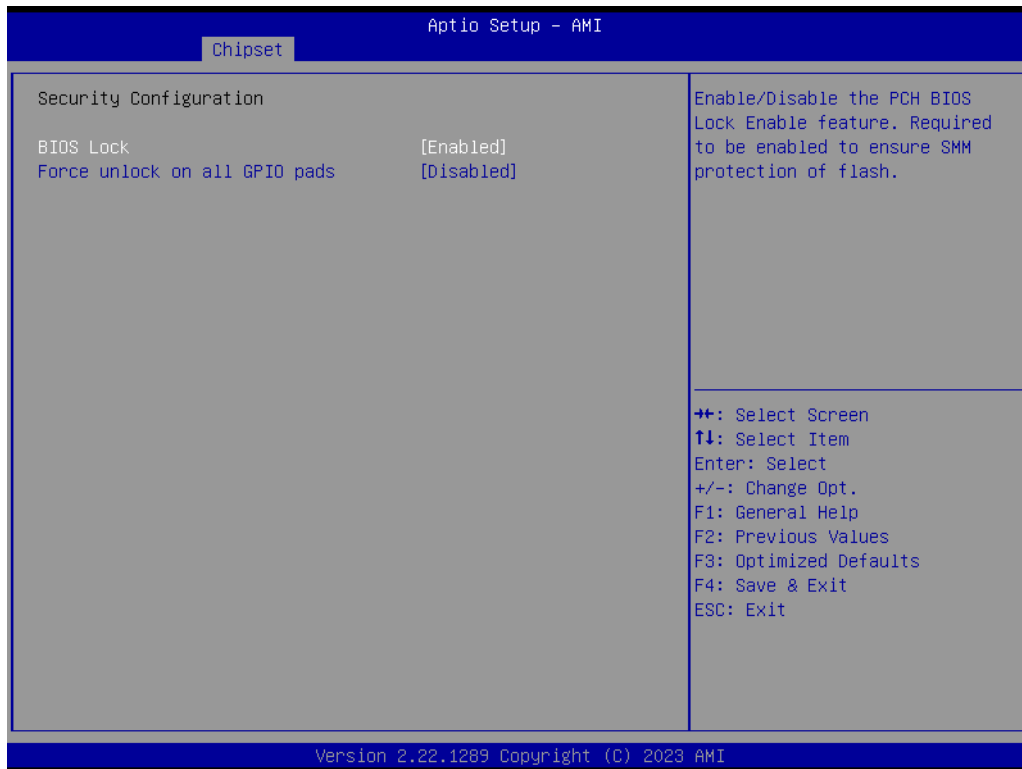


Figure 3.35 USB Configuration

- **xDCI Support**  
Enable/Disable xDCI (USB OTG Device).
- **USB Port Disable Override**  
Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.



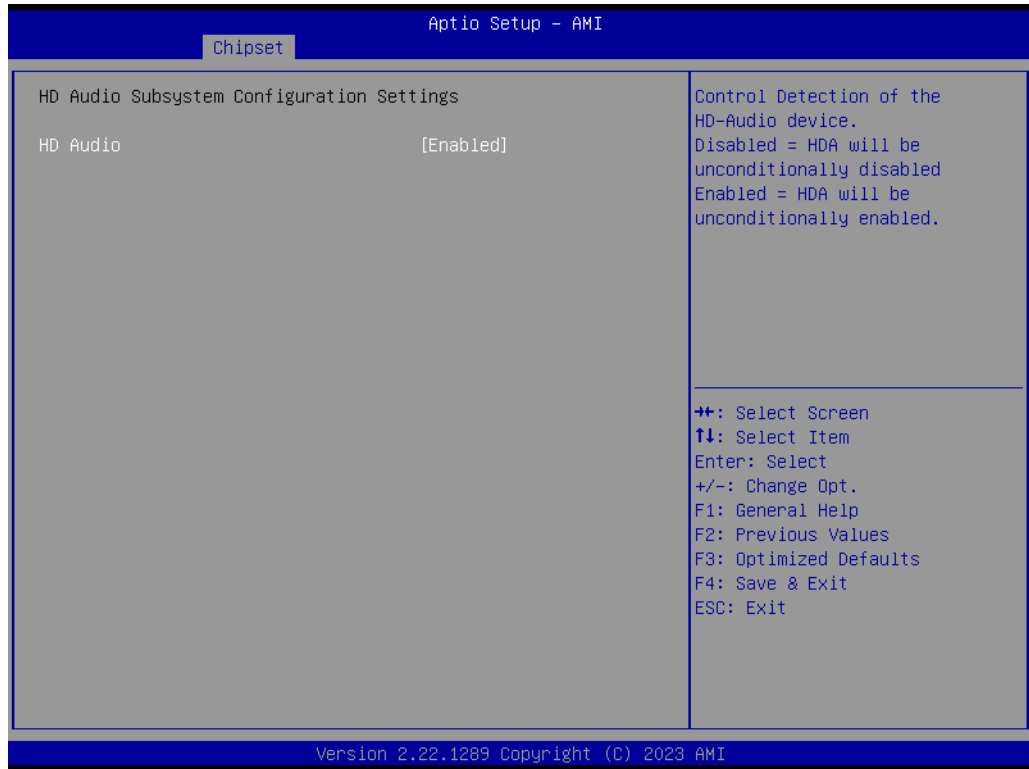
### 3.5.2.4 Security Configuration



**Figure 3.36 Security Configuration**

- **BIOS Lock**  
Enable/Disable the PCH BIOS Lock Enable feature. It is required to be enabled to ensure SMM protection of flash.
- **Force unlock on all GPIO pads**  
If Enabled, BIOS will force all GPIO pads to be in the unlocked state.

### 3.5.2.5 HD Audio Subsystem Configuration Settings



**Figure 3.37 HD Audio Subsystem Configuration Settings**

- **HD Audio**  
Control Detection of the HD-Audio device. Disabled=HDA will be unconditionally disabled. Enabled=HDA will be unconditionally enabled.

### 3.5.2.6 SerialIo Configuration



**Figure 3.38 SerialIo Configuration**

- **I2C2 Controller**  
 Enable/Disable SerialIo Controller.  
 If a given device's Function 0 PSF disabling is skipped, the PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.  
 The following devices depend on each other:  
 I2C0 and I2C1,2,3  
 UART0 and UART1,SPI0,1  
 UART2 and I2C4,5

UART 0 (00:30:00) cannot be disabled when:  
 1. Child device is enabled like CNVi Bluetooth (\\_SB.PC00.UA00.BTH0)

UART 0 (00:30:00) cannot be enabled when:  
 1. I2S Audio codec is enabled (\\_SB.PC00.I2C0.HDAC)
- **I2C4 Controller**  
 Enable/Disable SerialIo Controller. For I2C5 and UART2 to work, this device has to be enabled.
- **SPIO Controller**  
 Enable/Disable SerialIo Controller.  
 If a given device's Function 0 PSF disabling is skipped, the PSF default will remain and device PCI CFG Space will still be visible. This is needed to allow PCI enumerator access functions above 0 in a multifunction device.  
 The following devices depend on each other:  
 I2C0 and I2C1,2,3  
 UART0 and UART1,SPI0,1  
 UART2 and I2C4,5

UART 0 (00:30:00) cannot be disabled when:  
 1. Child device is enabled like CNVi Bluetooth (\\_SB.PC00.UA00.BTH0)

UART 0 (00:30:00) cannot be enabled when:

1. I2S Audio codec is enabled (\\_SB.PC00.I2C0.HDAC)

- **UART0 Controller**

Set UART0 mode – DBG used for BIOS log print and/or Kernel OS Debug – COM – 16550 compatible serial port with Power Gating support.

- **Serial IO I2C2 Settings**

Configure SerialIO Controller.

- **Serial IO I2C4 Settings**

Configure SerialIO Controller.

- **Serial IO UART0 Settings**

Configure SerialIO Controller.

- **SerialIO timing parameters**

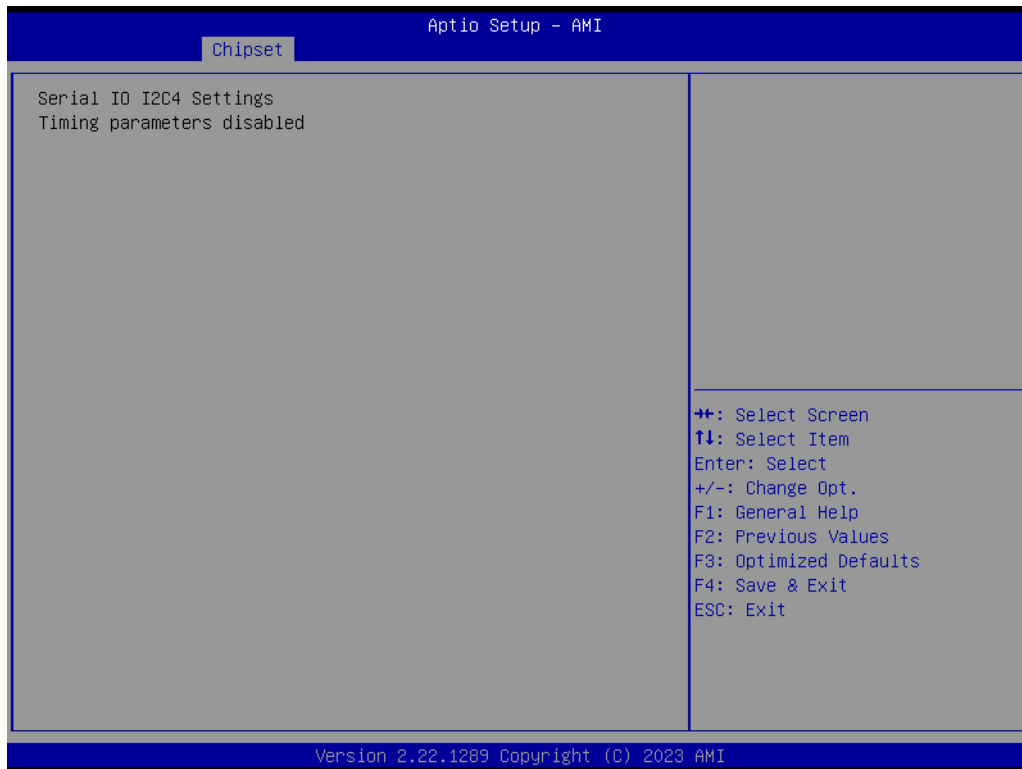
Enables additional timing parameters for all SerialIO controllers. Defaults can be changed in each controller setting. A platform restart is required to apply changes.

- **Serial IO I2C2 Settings**



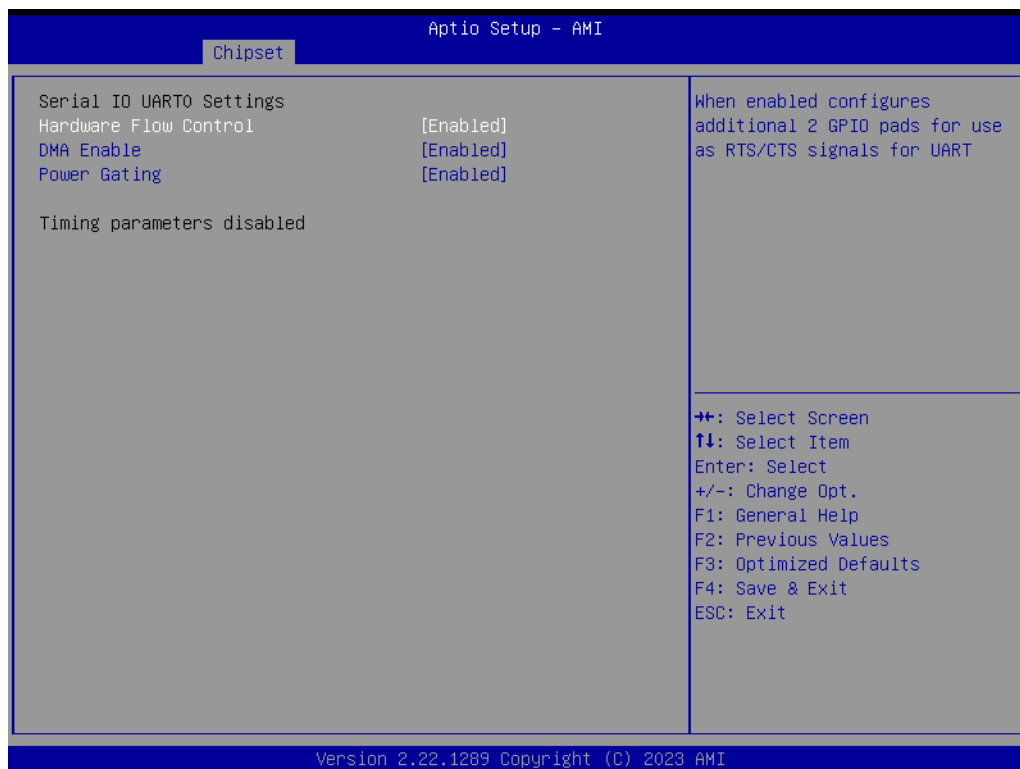
**Figure 3.39 Serial IO I2C2 Settings**

## Serial IO I2C4 Settings



**Figure 3.40 Serial IO I2C4 Settings**

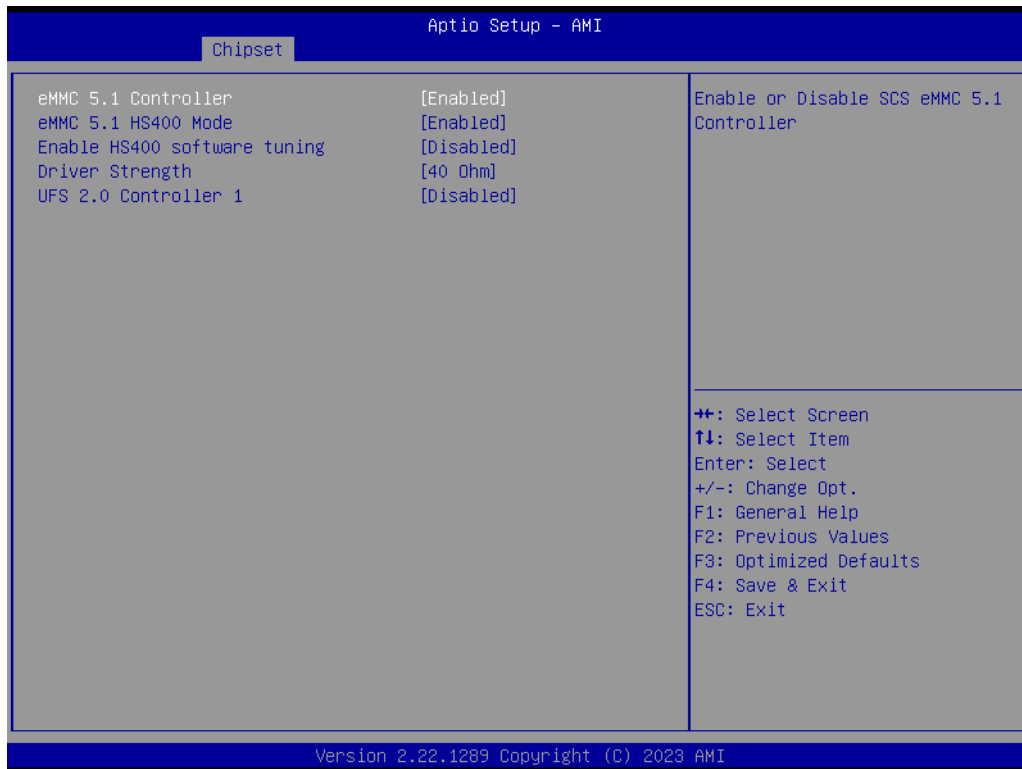
## ■ Serial IO UART0 Settings



**Figure 3.41 Serial IO UART0 Settings**

- **Hardware Flow Control**  
When enabled, it configures an additional 2 GPIO pads for use as RTS/CTS signals for UART.
- **DMA Enable**  
Enabled: The UART OS driver will use DMA when possible. Disabled: The OS driver will enforce PIO mode.
- **Power Gating**  
Disabled: No `_PS0` `_PS3` support, device is left in D0, after initialization  
Enabled: `_PS0` `_PS3` supports getting the device out of reset Auto: `_PS0` and `_PS3` detection through ACPI if the device was initialized prior to first PG. If it was used, (DBG2) PG is disabled.

### 3.5.2.7 SCS Configuration



**Figure 3.42 SCS Configuration**

- **eMMC 5.1 Controller**  
Enable or Disable the SCS eMMC 5.1 Controller.
- **eMMC 5.1 HS400 Mode**  
Enable or Disable SCS eMMC 5.1 HS400 Mode.
- **Enable HS400 software tuning**  
Software tuning should improve eMMC HS400 stability at the expense of boot time.
- **Driver Strength**  
Sets I/O driver strength.
- **UFS 2.0 Controller 1**  
Enable or Disable the UFS 2.0 Controller.

## 3.6 Security Chipset

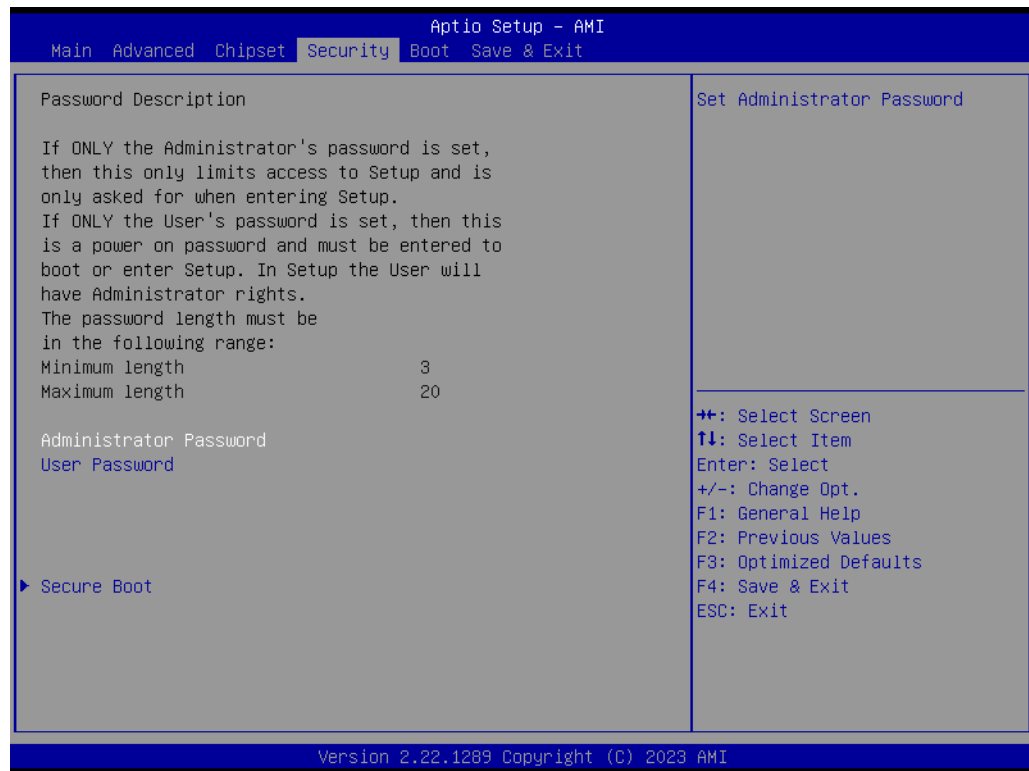


Figure 3.43 Security Chipset

- **Administrator Password**  
Set Setup Administrator Password.
- **User Password**  
Set User Password.
- **Secure Boot**  
Secure Boot Configuration.



### 3.6.1 Secure Boot



**Figure 3.44 Secure Boot**

- **Secure Boot**  
The Secure Boot feature is Active if Secure Boot is Enabled. Platform Key (PK) is enrolled and the System is in User mode. The mode change requires a platform reset.
- **Secure Boot Mode**  
Secure Boot mode options:  
Standard or Custom.  
In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.

## 3.7 Boot Setup

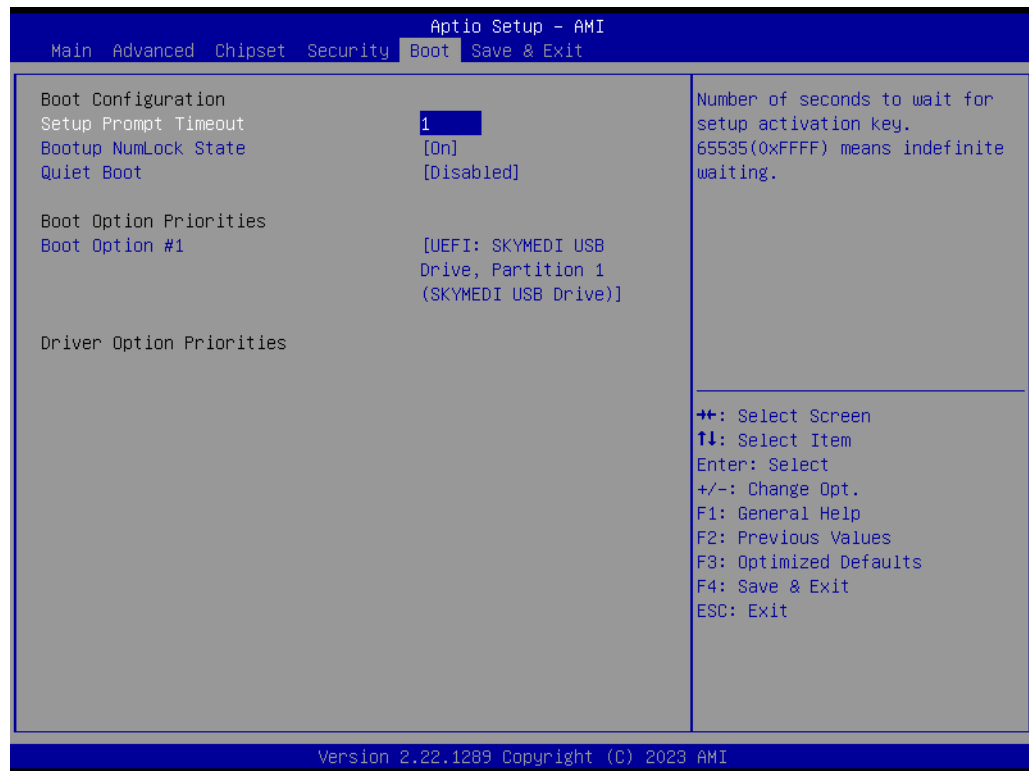
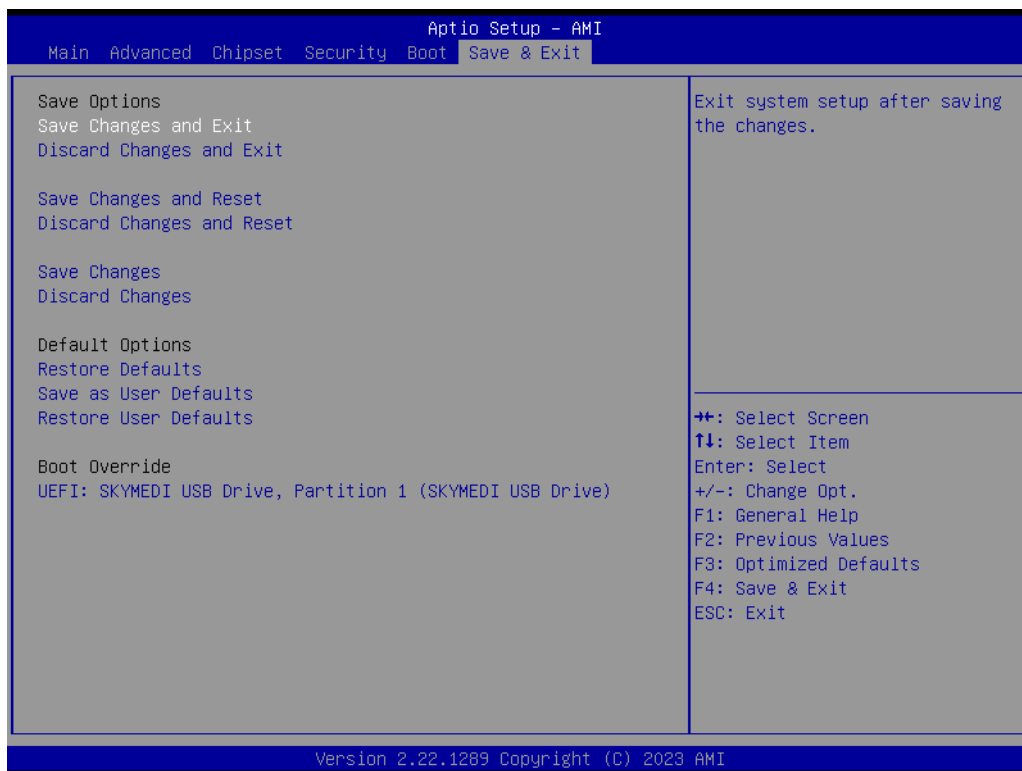


Figure 3.45 Boot Setup

- **Setup Prompt Timeout**  
Number of seconds to wait for the setup activation key. 65535(0xFFFF) means indefinite waiting.
- **Bootup NumLock State**  
Select the keyboard NumLock state.
- **Quiet Boot**  
Enable or Disable the Quiet Boot option.
- **Boot Option #1**  
Sets the system boot order.

## 3.8 Save & Exit



**Figure 3.46 Save & Exit**

- **Save Changes and Exit**  
Exit system setup after saving the changes.
- **Discard Changes and Exit**  
Exit system setup without saving any changes.
- **Save Changes and Reset**  
Reset the system after saving the changes.
- **Discard Changes and Reset**  
Reset system setup without saving any changes.
- **Save Changes**  
Save changes done so far to any of the setup options.
- **Discard Changes**  
Discard changes done so far to any of the setup options.
- **Restore Defaults**  
Restore/Load default values for all the setup options.
- **Save as User Defaults**  
Save the changes done so far as User Defaults.
- **Restore User Defaults**  
Restore the user defaults to all the setup options.
- **Boot Override**



# Chapter 4

## S/W Introduction & Installation

- S/W Introduction
- Driver Installation
- Advantech iManager

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## 4.1 S/W Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft Windows embedded technology." We enable Windows Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (Hardware suppliers, System integrators, Embedded OS distributor) for projects. Our goal is to make Windows Embedded Software solutions easily and widely available to the embedded computing community.

## 4.2 Driver Installation

The Intel Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured.

### 4.2.1 Windows Driver Setup

To install the drivers on a windows-based operating system, please connect to the Internet and go to the website <http://support.advantech.com.tw> to download the drivers that you want to install and follow the Driver Setup instructions to complete the installation.

### 4.2.2 Other OS

Linux Ubuntu and Yocto.

## 4.3 Advantech iManager

Advantech's platforms come equipped with iManager, a micro-controller that provides embedded features for system integrators. Embedded features have been moved from the OS/BIOS level to the board level to increase reliability and simplify integration. iManager runs whether the operating system is running or not; it can count the boot times and running hours of the device, monitor device health, and provide an advanced watchdog to handle errors just as they happen. iManager also comes with a secure and encrypted EEPROM for storing important security keys or other customer-defined information. All the embedded functions are configured through API and provide corresponding utilities to demonstrate. These APIs comply with PICMG EAPI (Embedded Application Programmable Interface) specifications and unify in the same structures. It makes these embedded features easier to integrate, speeding up development schedules and providing the customers with software continuity when upgrading hardware. For more details on how to use the APIs and utilities, please refer to the Advantech iManager 2.0 Software API User Manual.

### Control



**GPIO**

General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off a device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.



**SMBus**

SMBus is the System Management Bus defined by Intel® Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface an embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.



**I2C**

I2C is a bi-directional two wire bus that was developed by Philips for use in their televisions in the 1980s. The I2C API allows a developer to interface with an embedded system environment and transfer serial messages using the I2C protocols, allowing multiple simultaneous device control.

### Display



**Brightness Control**

The Brightness Control API allows a developer to interface with an embedded device to easily control brightness.



**Backlight**

The Backlight API allows a developer to control the backlight (screen) on/off in an embedded device.

### Monitor



**Watchdog**

A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.



**Hardware Monitor**

The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature and voltage.



**Hardware Control**

The Hardware Control API allows developers to set the PWM (Pulse Width Modulation) value to adjust fan speed or other devices; it can also be used to adjust the LCD brightness.

### Power Saving



**CPU Speed**

Make use of Intel SpeedStep technology to reduce power power consumption. The system will automatically adjust the CPU Speed depending on system loading.



**System Throttling**

Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. These APIs allow the user to lower the clock from 87.5% to 12.5%.





# Appendix **A**

## Pin Assignment

This appendix gives you the information about the hardware pin assignments for the SOM-7533 CPU System on Module.

Sections include:

- SOM-7533 Type 10 Pin Assignment

## A.1 SOM-7533 Pin Assignment

This section shows the SOM-7533 pin assignment on the COM Express connector, which is compliant with COMR.0 R3.1 Type 10 pin-out definitions. For more details about how to use these pins and for design reference, please contact Advantech for a design guide, checklist, reference schematic, and other hardware/software support.

**Table A.1: SOM-7533 Rows A, B**

A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK1G#	B4	LPC_AD0
A5	GBE0_LINK2.5#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	ESPI_ALERT1#
A9	GBE0_MDI1-	B9	N/A
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	N/A	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	N/A
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	USB_SSRX0-	B22	USB_SSTX0-
A23	USB_SSRX0+	B23	USB_SSTX0+
A24	SUS_S5#		
B24	PWR_OK		
A25	USB_SSRX1-	B25	USB_SSTX1-
A26	USB_SSRX1+	B26	USB_SSTX1+
A27	BATLOW#	B27	WDT
A28	(S)ATA_ACT#	B28	N/A
A29	AC/HDA_SYNC	B29	AC/HDA_SDIN1
A30	AC/HDA_RST#	B30	AC/HDA_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC/HDA_BITCLK	B32	SPKR
A33	AC/HDA_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-

Table A.1: SOM-7533 Rows A, B			
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	ESPI_EN#
A48	CB_RSMRST#	B48	N/A
A49	LAN0_SDP0	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#(PLTRST#)
A51	GND (FIXED)	B51	GND (FIXED)
A52	RSVD	B52	RSVD
A53	RSVD	B53	RSVD
A54	GPI0		
B54	GPO1		
A55	GP_SPI_CS#	B55	GP_SPI_MISO
A56	GP_SPI_CK	B56	GP_SPI_MOSI
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+	B71	DDIO_PAIR0+
A72	LVDS_A0-	B72	DDIO_PAIR0-
A73	LVDS_A1+	B73	DDIO_PAIR1+
A74	LVDS_A1-	B74	DDIO_PAIR1-
A75	LVDS_A2+	B75	DDIO_PAIR2+
A76	LVDS_A2-	B76	DDIO_PAIR2-
A77	LVDS_VDD_EN	B77	N/A
A78	LVDS_A3+	B78	N/A
A79	LVDS_A3-	B79	eDP_BKLT_EN
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+	B81	DDIO_PAIR3+
A82	LVDS_A_CK-	B82	DDIO_PAIR3-
A83	LVDS_I2C_CK	B83	eDP_BKLT_CTRL
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY

**Table A.1: SOM-7533 Rows A, B**

A86	RSVD	B86	VCC_5V_SBY
A87	eDP_HPDP	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A89	PCIE0_CK_REF-	B89	DDIO_HPDP
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	N/A
A92	SPI_MISO	B92	N/A
A93	GPO0	B93	N/A
A94	SPI_CLK	B94	N/A
A95	SPI_MOSI	B95	DDIO_DDC_AUX_SEL
A96	TPM_PP	B96	N/A
A97	TYPE10#		
B97	SPI_CS#		
A98	SER0_TX	B98	DDIO_CTRLCLK_AUX+
A99	SER0_RX	B99	DDIO_CTRLDATA_AUX-
A100	GND (FIXED)	B100	GND (FIXED)
A101	SER1_TX	B101	FAN_PWMOUT
A102	SER1_RX	B102	FAN_TACHIN
A103	LID#	B103	SLEEP#
A104	VCC_12V		
B104	VCC_12V		
A105	VCC_12V		
B105	VCC_12V		
A106	VCC_12V		
B106	VCC_12V		
A107	VCC_12V		
B107	VCC_12V		
A108	VCC_12V		
B108	VCC_12V		
A109	VCC_12V		
B109	VCC_12V		
A110	GND (FIXED)	B110	GND (FIXED)

**\*Note:**

1. A50 could be an optional pin reserved for ESPI\_CS1#. Please contact FAE for details.
2. A71 could be an optional pin reserved for eDP\_TX2+. Please contact FAE for details.
3. A72 could be an optional pin reserved for eDP\_TX2-. Please contact FAE for details.
4. A73 could be an optional pin reserved for eDP\_TX1+. Please contact FAE for details.
5. A74 could be an optional pin reserved for eDP\_TX1-. Please contact FAE for details.
6. A75 could be an optional pin reserved for eDP\_TX0+. Please contact FAE for details.
7. A76 could be an optional pin reserved for eDP\_TX0-. Please contact FAE for details.

8. A77 could be an optional pin reserved for eDP\_VDD\_EN. Please contact FAE for details.
9. A81 could be an optional pin reserved for eDP\_TX3+. Please contact FAE for details.
10. A82 could be an optional pin reserved for eDP\_TX3-. Please contact FAE for details.
11. A83 could be an optional pin reserved for eDP\_AUX+. Please contact FAE for details.
12. A84 could be an optional pin reserved for eDP\_AUX-. Please contact FAE for details.
13. A101 could be an optional pin reserved for EC CAN0\_TX. Please contact FAE for details.
14. A102 could be an optional pin reserved for EC CAN0\_RX. Please contact FAE for details.
15. B3 could be an optional pin reserved for ESPI\_CS0#. Please contact FAE for details.
16. B4 could be an optional pin reserved for ESPI\_IO\_0. Please contact FAE for details.
17. B5 could be an optional pin reserved for ESPI\_IO\_1. Please contact FAE for details.
18. B6 could be an optional pin reserved for ESPI\_IO\_2. Please contact FAE for details.
19. B7 could be an optional pin reserved for ESPI\_IO\_3. Please contact FAE for details.
20. B8 could be an optional pin reserved for ESPI\_ALERT0#. Please contact FAE for details.
21. B10 could be an optional pin reserved for ESPI\_CLK. Please contact FAE for details.
22. B18 could be an optional pin reserved for ESPI\_RESET#. Please contact FAE for details.
23. B79 could be an optional pin reserved for eDP\_BKLT\_EN. Please contact FAE for details.
24. B83 could be an optional pin reserved for eDP\_BKLT\_CTRL. Please contact FAE for details.



# Appendix **B**

## Watchdog Timer

This appendix gives you information about programming the watchdog timer on the SOM-7533 CPU System on Module.

Sections include:

- Watchdog Timer Programming

## B.1 Programming the Watchdog Timer

**Table B.1: Programming the Watchdog Timer**

Trigger Event	Note
IRQ	(BIOS setting default disable)**
NMI	N/A
SCI	Power button event
Power Off	Support
H/W Restart	Support
WDT Pin Activate	Support

\*\* WDT new driver support automatically selects an available IRQ number from the BIOS, and then sets it to EC. Only Win10 supports it.

In other OS, it will still use the IRQ number from the BIOS settings as usual.

For details, please refer to iManager and the Software API User Manual.



# Appendix **C**

## Programming GPIO

This appendix illustrates the General Purpose Input and Output pin settings.

Sections include:

- GPIO Register

## C.1 GPIO Register

**Table C.1: GPIO Register**

<b>GPIO Byte Mapping</b>	<b>H/W Pin Name</b>
BIT0	GPI0
BIT1	GPI1
BIT2	GPI2
BIT3	GPI3
BIT4	GPO0
BIT5	GPO1
BIT6	GPO2
BIT7	GPO4

For details, please refer to iManager and the Software API User Manual.

# Appendix **D**

## System Assignments

This appendix gives you information about system resource allocation on the SOM-7533 CPU System on Module.

Sections include:

- System I/O Ports
- DMA Channel Assignments
- Interrupt Assignments
- 1<sup>st</sup> MB Memory Map

## D.1 System I/O Ports

**Table D.1: System I/O Ports**

<b>Addr.Range(Hex)</b>	<b>Device</b>
0x00000299-0x0000029A	Motherboard resources
0x000002C0-0x000002DF	Motherboard resources
0x000002A0-0x000002BF	Motherboard resources
0x000002A0-0x000002BF	Motherboard resources
0x00000290-0x0000029F	Motherboard resources
0x0000029E-0x000002AD	Motherboard resources
0x00000060-0x0000006F	Motherboard resources
0x00000200-0x0000027F	Motherboard resources
0x00000300-0x0000037F	Motherboard resources
0x00000280-0x0000028F	Motherboard resources
0x00000280-0x0000028F	Motherboard resources
0x000002F0-0x000002F7	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000068-0x00000069F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x00000062-0x00000062	Microsoft ACPI-Compliant Embedded Controller
0x00000066-0x00000066	Microsoft ACPI-Compliant Embedded Controller
0x00001854-0x00001857	Motherboard resources
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller

**Table D.1: System I/O Ports**

0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x00003000-0x0000303F	Intel® UHD Graphics
0x00000000-0x00000CF7	PCI Express Root Complex
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x00003090-0x00003097	Standard SATA AHCI Controller
0x00003080-0x00003083	Standard SATA AHCI Controller
0x00003060-0x0000307F	Standard SATA AHCI Controller
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer
0x00002000-0x000020FE	Motherboard resources

## D.2 Interrupt Assignments

**Table D.2: Interrupt Assignments**

<b>Interrupt#</b>	<b>Interrupt Source</b>
IRQ 0	System timer
IRQ 14	Intel® Serial IO GPIO Host Controller - INTC1057
IRQ 16	Intel SD Host Controller
IRQ 16	Intel® Serial IO UART Host Controller - 54A8
IRQ 17	USB Synopsys Controller
IRQ 256-511	Microsoft ACPI-Compliant System
IRQ 27	Intel® Serial IO I2C Host Controller - 54E8
IRQ 29	Intel® Serial IO I2C Host Controller - 54EA
IRQ 3	Communications Port (COM2)
IRQ 31	Intel® Serial IO I2C Host Controller - 54C5
IRQ 4	Communications Port (COM1)
IRQ 4294967279	Intel® Management Engine Interface #1
IRQ 4294967280	Intel® Smart Sound Technology BUS
IRQ 4294967281-4294967289	Intel® Ethernet Controller I226-LM #3
IRQ 4294967290	Intel® USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
IRQ 4294967291	Intel® UHD Graphics
IRQ 4294967292	Standard SATA AHCI Controller
IRQ 4294967293	PCI Express Root Port #1 - 54B8
IRQ 4294967294	PCI Express Root Port #7 - 54BE
IRQ 55-204	Microsoft ACPI-Compliant System
IRQ 6	Motherboard resources

## D.3 1st MB Memory Map

**Table D.3: 1st MB Memory Map**

Addr. Range (Hex)	Device
0xFEDC0000-0xFEDC7FFF	Motherboard resources
0xFEDA0000-0xFEDA0FFF	Motherboard resources
0xFEDA1000-0xFEDA1FFF	Motherboard resources
0xC0000000-0xCFFFFFFF	Motherboard resources
0xFED20000-0xFED7FFFF	Motherboard resources
0xFED90000-0xFED93FFF	Motherboard resources
0xFED45000-0xFED8FFFF	Motherboard resources
0xFEE00000-0xFEEFFFFFFF	Motherboard resources
0x80400000-0x806FFFFF	PCI Express Root Port #7 - 54BE
0x80400000-0x806FFFFF	PCI Express Root Complex
0xFFCF7000-0xFFCF7FFF	Intel® Management Engine Interface #1
0xFFCF9000-0xFFCF9FFF	Intel® Serial IO I2C Host Controller - 54E8
0x80500000-0x805FFFFF	Intel® Ethernet Controller I226-LM #3
0x80600000-0x80603FFF	Intel® Ethernet Controller I226-LM #3
0xFED00000-0xFED003FF	High precision event timer
0xFFCFC000-0xFFCFFFFFFF	Intel® Smart Sound Technology BUS
0xFFD00000-0xFFDFFFFFFF	Intel® Smart Sound Technology BUS
0xFFE00000-0xFFFFFFFFFFF	USB Synopsys Controller
0xFFCFA000-0xFFCFAFFF	USB Synopsys Controller
0x0000-0xFFFFFFF	Intel® UHD Graphics
0x0000-0xFFFFFFF	Intel® UHD Graphics
0xFFCF6000-0xFFCF6FFF	Intel® Serial IO I2C Host Controller - 54C5
0xFFCFB000-0xFFCFBFFF	Intel® Serial IO UART Host Controller - 54A8
0xA0000-0xBFFFF	PCI Express Root Complex
0xE0000-0xE3FFF	PCI Express Root Complex
0xE4000-0xE7FFF	PCI Express Root Complex
0xE8000-0xEBFFF	PCI Express Root Complex
0xEC000-0xEFFFF	PCI Express Root Complex
0xF0000-0xFFFFF	PCI Express Root Complex
0x80700000-0x80701FFF	Standard SATA AHCI Controller
0x80703000-0x807030FF	Standard SATA AHCI Controller
0x80702000-0x807027FF	Standard SATA AHCI Controller
0xFED40000-0xFED44FFF	Trusted Platform Module 2.0
0x1300000-0x130FFFF	Intel® USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
0xFD6E0000-0xFD6EFFFF	Intel® Serial IO GPIO Host Controller - INTC1057
0xFD6D0000-0xFD6DFFFF	Intel® Serial IO GPIO Host Controller - INTC1057
0xFD6A0000-0xFD6AFFFF	Intel® Serial IO GPIO Host Controller - INTC1057
0xFD690000-0xFD69FFFF	Intel® Serial IO GPIO Host Controller - INTC1057
0x132A000-0x132AFFF	Intel SD Host Controller
0xFFCF8000-0xFFCF8FFF	Intel® Serial IO I2C Host Controller - 54EA
0x1310000-0x1317FFF	Performance Monitor
0xFE010000-0xFE010FFF	SPI (flash) Controller - 54A4



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