User Manual

iDAQ Chassis (iDAQ-934 & iDAQ-964)

ADVANTECH

Enabling an Intelligent Planet

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5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

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Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

Test conditions for passing also include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference. In this event, users are required to correct the interference at their own expense.

Technical Support and Assistance

1. Visit the Advantech website at www.advantech.com/support to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions, and Notes

Warning! *Warnings indicate conditions that if not observed can cause personal injury!*

Caution! *Cautions are included to help prevent hardware damage and data losses. For example,*

"Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions."

Note! *Notes provide additional optional information.*

Document Feedback

To assist us with improving this manual, we welcome all comments and constructive criticism. Please send all feedback in writing to support@advantech.com.

Packing List

Before system installation, check that the items listed below are included and in good condition. If any item does not accord with the list, contact your dealer immediately.

iDAQ-934

- iDAQ-934 x 1
- USB 3.0 Cable x 1
- 2-pin connector x 1
- DIN-Rail Kit x 2 (each set has screws x 2, frame x 1, buckle x 1)
- Startup Manual x 1

iDAQ-964

- iDAQ-964 x 1
- Screw x 3
- Startup Manual x 1

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from all power outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If any of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated the equipment.
    - The equipment has been exposed to moisture.
    - The equipment is malfunctioning, or does not operate according to the user manual.
    - The equipment has been dropped and damaged.
    - The equipment shows obvious signs of breakage.
15. Do not leave the equipment in an environment with a storage temperature of below -20° C (-4° F) or above 60° C (140° F) as this may damage the components. The equipment should be kept in a controlled environment.
16. CAUTION: Batteries are at risk of exploding if incorrectly replaced. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
17. In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator's position does not exceed 70 dB (A).

DISCLAIMER: These instructions are provided according to IEC 704-1 standards. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precautions - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.
- Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

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Chapter 1

Start Using iDAQ Chassis

1.1 Overview

This chapter provides an overview of Advantech industrial data acquisition (iDAQ) chassis for iDAQ-934 and iDAQ-964, its features and accessories.

iDAQ-934 is a four-slot data acquisition chassis with robust design for use with iDAQ modules. Various analog and digital I/O signals can be measured or output when using with the corresponding iDAQ modules. Acquisition among multiple iDAQ modules can be synchronized by the internal acquisition engines for a better precision measurements. Data are transferred to or from the host computer through a SuperSpeed USB 3.0 interface.

iDAQ-964 on the other hand, is a four-slot data acquisition chassis with similar design as iDAQ-934. It's a chassis module to realize the availability of iDAQ functionalities on the AMAX-5000 platform. (For the actual AMAX model, please refer to AMAX series product portfolio.)

1.2 Product Overview

IDAQ-934

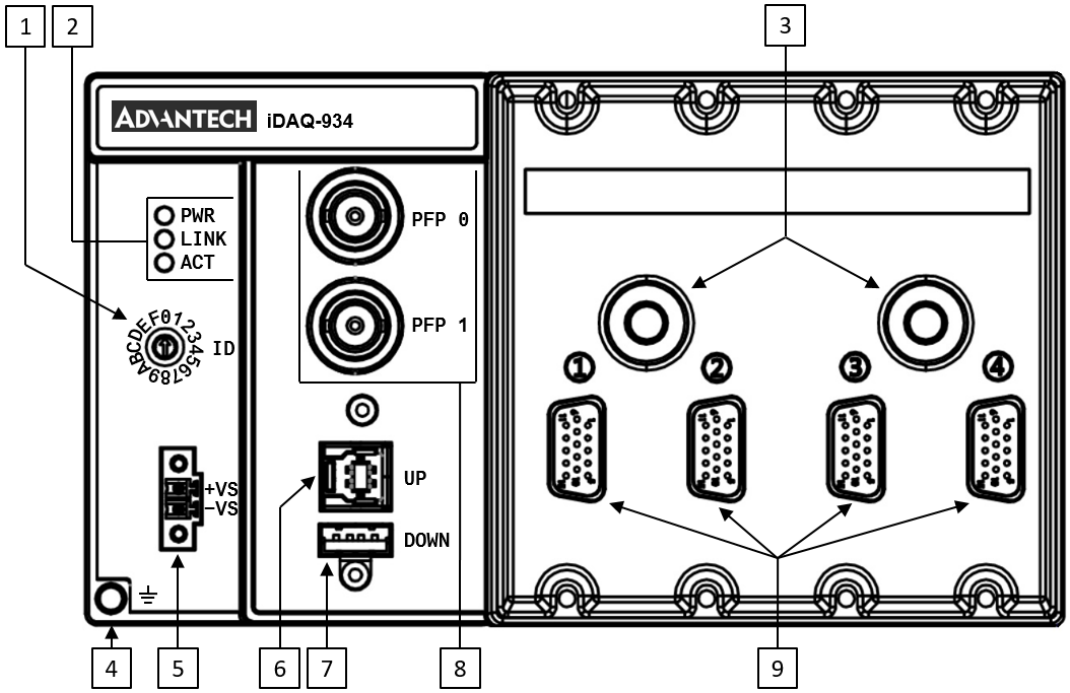


Figure 1.1 Front View of iDAQ-934

Number	Component
1	Board ID rotary switch
2	LED indicators
3	Holes for panel mount
4	Chassis grounding screw
5	Power input connector
6	Upstream USB port connector
7	Downstream USB port connector
8	Programmable function pin (PFP) BNC connectors
9	Slots for iDAQ modules

IDAQ-964

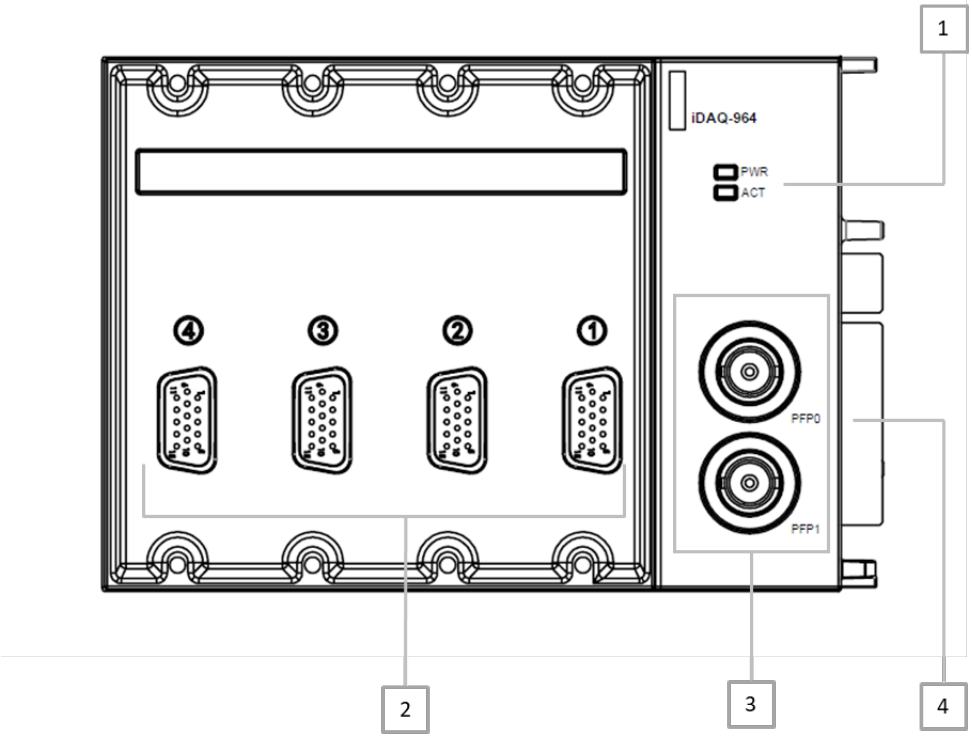


Figure 1.2 Front View of iDAQ-964

Number	Component
1	LED indicators
2	Slots for iDAQ modules
3	Programmable function pin (PFP) BNC connectors
4	PCI Express interface

1.3 Product Features

1.3.1 Power Input

The iDAQ chassis requires an external power supply to operate. Connect the external power supply to the 2-pin spring terminal, and insert the terminal to the power input connector. Refer to 2.4.2 for the pin assignment of the terminal and A.7 for the required supply voltage and power rating.

1.3.2 Upstream USB Port

Use the lockable USB 3.0 cable in the package to connect the USB type-B connector on the iDAQ chassis to a SuperSpeed USB 3.0 port on the host computer, and lock the cable to the iDAQ chassis with a screw. A Hi-Speed USB 2.0 port on the host computer can also be used, but not recommended. Acquisition speed may be limited when using a Hi-Speed USB 2.0 port.

The iDAQ chassis only draws minimum current from the upstream port. External power supply is required for operation. Refer to A.7 for detailed specifications.

1.3.3 Downstream USB Port

There is an USB 3.0 hub controller inside the iDAQ chassis, which provides another general purpose SuperSpeed USB 3.0 port for downstream extension. Any USB device can be connected to this port, such as another iDAQ chassis. This type-A connector also provides a screw hole for use on the lockable USB cable.

1.3.4 LED Indicators

The LED indicators shows the operational status of the iDAQ chassis. Refer to 3.7 Status Indication for detailed description.

1.3.5 Programmable Function Pin (PFP)

The programmable function pins provide bi-directional, multi-function signals. External trigger or clock signals can be fed into PFP pins for acquisition timing control. The internal trigger or clock signals can also be routed and output to PFP pins for external use, such as synchronizing multiple iDAQ chassis. Refer to section A6 for detailed specifications and section 3.6 for pin definition.

1.3.6 Slots for IDAQ Modules

Each slot of iDAQ systems accepts one iDAQ module. Insert the module and screw it to the chassis firmly using the two screws. Make sure both screws are on their threads before tightening.

The modules are hot swappable, which means they can be inserted into or removed from the slots freely even when the chassis is powered on. The software driver will detect the insertion and removal of the modules automatically. Before removing a module, however, be sure that no I/O-side power is connected to it.

For detailed installation instruction, please refer to 2.3.

1.3.7 Board ID

A board ID can be assigned to the iDAQ chassis by the rotary switch. The board ID will be shown in the software and can be used to distinguish each chassis. The number shown besides the rotary switch is in hexadecimal format. For example, “A” represent 10 in decimal format, and “F” represents 15 in decimal format. Refer to 3.8 for detailed description.

1.3.8 Chassis Grounding Screw

To ensure the specified EMC performance, the iDAQ chassis must be connected to the earth ground point through chassis grounding screw.

1.4 Driver Installation

The drivers for iDAQ chassis are included in drivers of iDAQ modules. You only need to install the drivers for iDAQ modules via XNavi installer, so that the iDAQ modules will be recognized by your system.

The driver package can be found on the Advantech Support Portal (https://www.advantech.com/support). Search for iDAQ on the support portal, then the corresponding driver/SDK package can be found. You'll get the XNavi installer after the download session finishes.

Execute the installer, then it will guide you through the session. You can choose the device and software components you'd like to install in the system (Figure 1.3). After the selection, click on "start" to begin the installation.

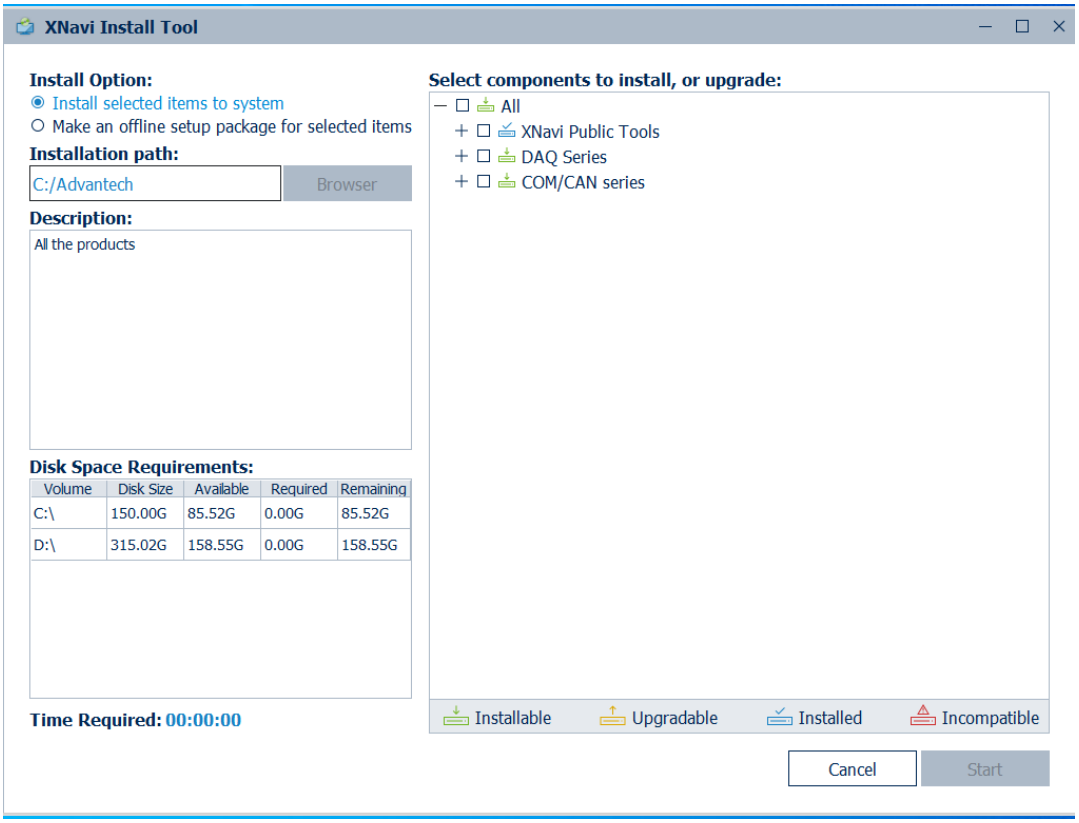


Figure 1.3 XNavi Installer

1.5 Software Utilities

Advantech offers device drivers, SDKs, third-party driver support and application software to help fully exploit the functions of your iDAQ system. All these software packages are available on Advantech website: http://www.advantech.com/.

The Advantech Navigator is a utility that allows you to set up, configure and test your device, and later stores your settings in a proprietary database.

1. To set up the I/O device for your card, you could first run the Advantech Navigator program (by accessing Start/Programs/Advantech Automation/DAQNavi/Advantech Navigator). The settings could also be saved.
2. You can then view the device(s) already installed on your system (if any) on the Installed Device tree view. If the software and hardware installation are completed, you will see iDAQ modules in the Installed Devices list.

1.6 Software Development Using DAQNavi SDK

DAQNavi SDK is the software development kit for programming applications with Advantech DAQ products. The necessary runtime DLL, header files, software manual and tutorial videos can be installed via XNavi installer. They can be found under C:\Advantech\DAQNavi (default directory) after the finishing the installation.

1.7 Application Software DAQNavi MCM

DAQNavi MCM is an application software focusing on high-speed data acquisition, data monitoring and network access. It provides a graphical interface for users to achieve DAQ configuration, data pre-processing, feature extraction, user-defined formula calculation and the output settings to upload data. All settings can also be saved to a project file for further parameter management. On top of that, the datalogging function is also available in DAQNavi/MCM. All data can be saved not only on local storage, but also in remote storage.

By introducing the DAQNavi/MCM, the DAQ system could become an IoT-solution-ready edge device. For more information, please search for DAQNavi/MCM on the Advantech Support Portal (https://www.advantech.com/support).

1.8 FPGA Code Download

The FPGA can also be updated via the interface in Navigator. However, it isn't the normal situation to move onto the FPGA update. Advantech strongly suggests you to consult your technical support before starting an FPGA update.

1.9 Accessories

PCL-1010B-1E	BNC Coax Cable, 1m
PSD-A40W12	DIN Rail AC to DC 100-240V 40W 12V
PSD-A40W24	DIN Rail AC to DC 100-240V 40W 24V

Chapter 2

Installation Guide

2.1 Installation

iDAQ-934

After the device drivers are installed, the iDAQ-934 chassis can be installed in the computer.

1. Touch any metal surface of the computer to discharge any static electricity that may be in your body.
2. Insert the USB cable into the designated USB port.

After the chassis and iDAQ modules are installed, the device can be configured using the Advantech Navigator Program automatically installed during driver setup. Note that the iDAQ modules would only be recognized when the module is inserted in the iDAQ chassis.

iDAQ-964

The iDAQ-964 should be used along with AMAX-5000 system. Here we take AMAX-5580 as an example. The assembly procedure is as follow:

1. Insert the PCI express BUS into the AMAX system.
2. Tighten the three screws around the connection on the AMAX-5580.

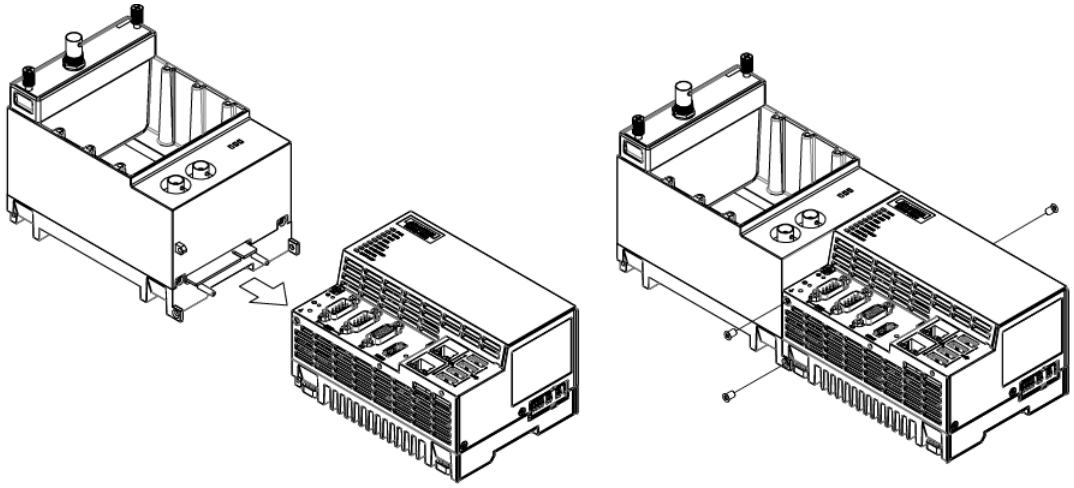


Figure 2.1 Installation Guide of iDAQ-964

2.2 Mounting

The iDAQ-934 provides two types of mounting method. One is DIN-rail and the other is wall mount.

2.2.1 DIN rail mount

The DIN Rail mounting kit is attached along with the package. Please make sure that the mounting kit is well-packed and components are completely included as follow:

- 2 x frames
- 2 x buckles
- 4 x screws

If anything is missing, please contact local sales representative or sales channel.

The assembly step is as following for the iDAQ-934:

1. Screw the two frames onto the chassis.
2. Insert the buckle into the frame respectively.

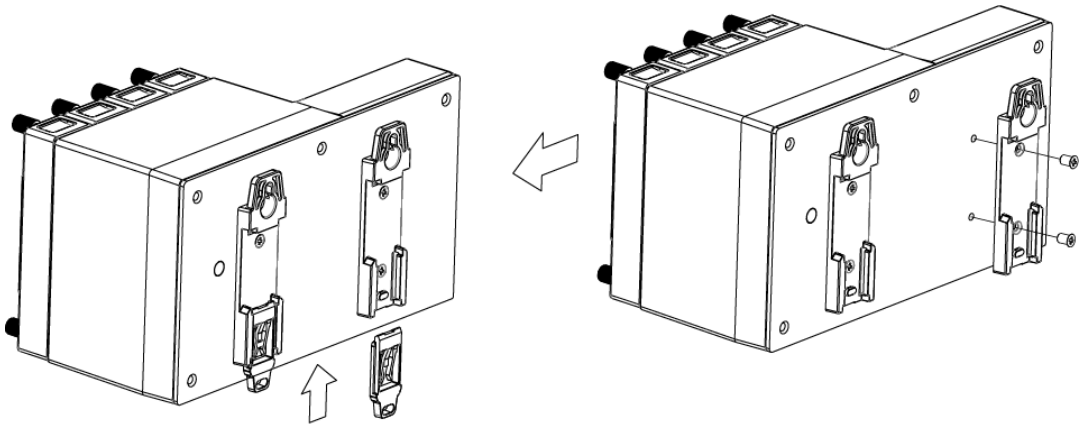


Figure 2.2 DIN-Rail assembly for iDAQ-934

2.2.2 Wall mount

There are two holes in the iDAQ-934 chassis module slot area. Those are the holes reserved for the wall mount. The following figures indicate the dimensions for mounting the iDAQ-934 chassis in a wall-mounting scenario. (unit: mm)

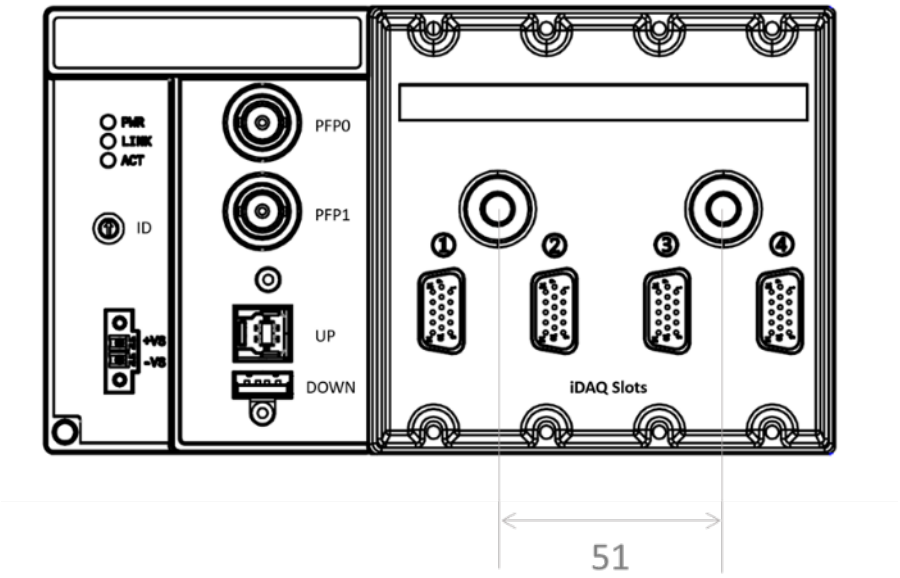


Figure 2.3 Wall-mount dimensions (1)

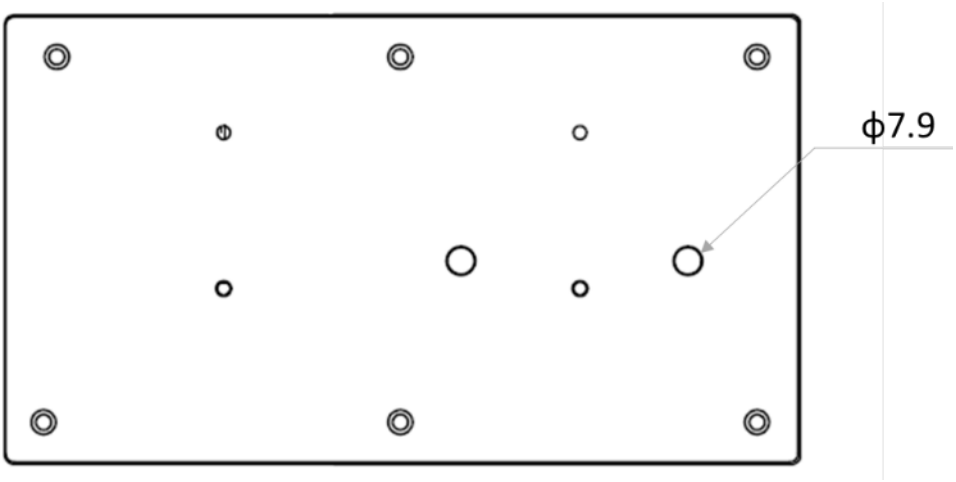


Figure 2.4 Wall-mount dimensions (2)

2.3 Using iDAQ Modules

Below are the steps to insert the iDAQ modules into the iDAQ chassis.

1. Insert the module following the guide rail to the end.
2. Screw the two screws tight onto the chassis, note that you should balance the depth of two screws when you screw them tightly.

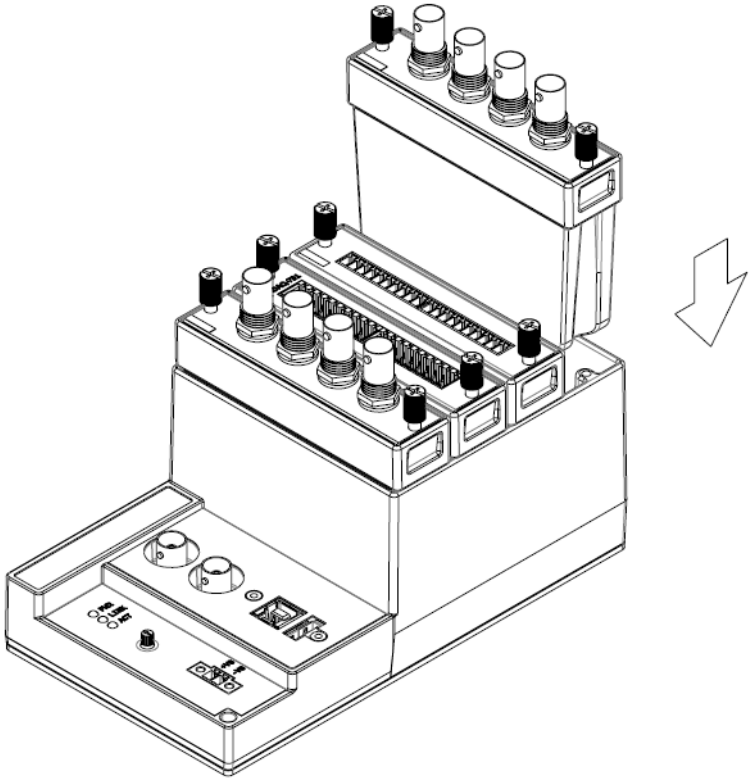


Figure 2.5 Installation of iDAQ modules

2.4 Signal Connection and Pin Definition

2.4.1 Programmable Function Pin Connector

The PFP stands for programmable function pin. It provides multiple functions such as clock I/O and trigger I/O. Refer to 3.1 and 3.6 for detailed application information, and also A6 for the signal specification.

Figure 2.6 Pin assignment of PFP connector

Pin Name	Description
PFP	Positive terminal of programmable function pin
GND	Ground. Negative terminal of programmable function pin

2.4.2 Power Connector

The iDAQ chassis uses a 2-pin connector as power connector for 10~30 V_{DC} power supply. The following is the description for the pins. For detailed specification regarding to power aspect, please refer to A7.

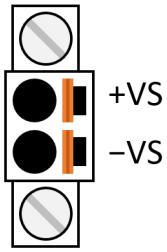


Figure 2.7 Pin assignment of power connector

Pin Name	Description
+VS	Positive terminal of power supply
−VS	Negative terminal of power supply

Note! *The iDAQ system is not a BUS-powered device. External power must be connected so that iDAQ system will perform correctly.*

Chapter 3

Function Details

Interface Introduction

3.1 Function Details

The iDAQ system relies on the chassis module as a platform to aggregate all the signals together, in order to achieve functions including synchronization, data streaming and timing control. This chapter describes all the functions that the iDAQ systems provide and how they work.

3.2 Trigger and Signal Routing

3.2.1 Signal Routing

When performing hardware-timed acquisition or update, the start and stop of the acquisition, and the timing for acquiring input samples and updating output samples are all controlled by an acquisition engine.

Each slot on iDAQ-934 has its own acquisition engine, which means every slot can use different timing signals (start trigger, stop trigger, and sample clock) to perform independent acquisition tasks. For example, one of the slots may be acquiring analog input data at 200 kS/s sample rate using an analog input module, and another slot may be acquiring digital input data at 10 kS/s sample rate using a digital input module. Each task can be started and stopped independently.

Each timing signal may come from one of various sources as shown in Figure 3.1. If multiple slots use the same source for timing signals, they can perform synchronized acquisition. The following sections describes the routing of these timing signals.

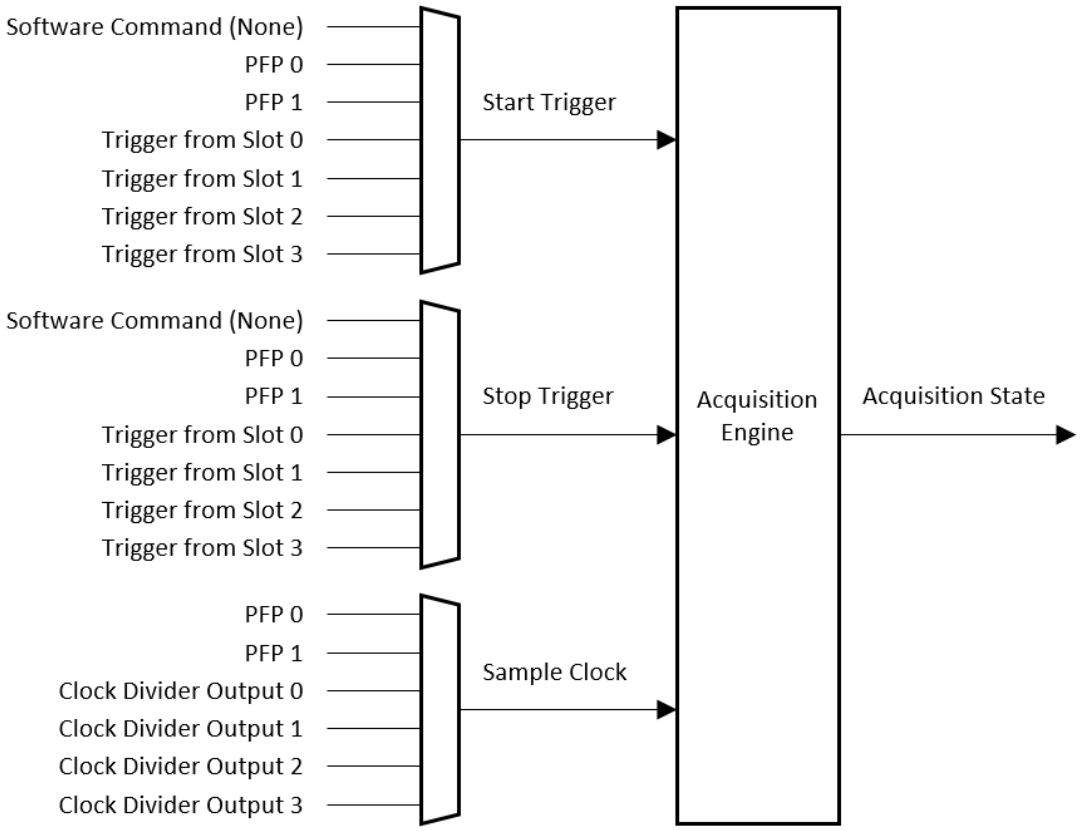


Figure 3.1 Signal routing of an acquisition engine.

There is also an acquisition state signal generated by the acquisition engine for inter-chassis synchronization.

3.2.2 Start Trigger and Stop Trigger

Start trigger and stop trigger may come from one of the following sources:

- Software command (choose “None” in the software)
- One of the programmable function pin (PFP) inputs
- Trigger from one of the slots

Trigger signals are edge sensitive. The active edge of the trigger source can be selected as rising edge active or falling edge active.

3.2.3 Sample Clock

Sample clock may come from one of the following sources:

- Programmable clock divider output
- One of the programmable function pin (PFP) inputs
- Signal from one of the slots

There is a programmable clock divider on the chassis for each acquisition engine. Refer to A.6 Acquisition Engine for possible output frequency.

Sample clock is always rising edge active.

3.2.4 Programmable Function Pin (PFP)

There are two programmable function pins (BNC connector) on the chassis. These pins are bi-directional and can be configured for various functions.

As an input pin, it can be the source of start trigger, stop trigger, or sample clock for an acquisition engine as shown in Figure 3.1.

As an output pin, the signal can come from one of the timing signals (start trigger, stop trigger, or sample clock) in one of the acquisition engines. This is shown in Figure 3.2 and 3.3.

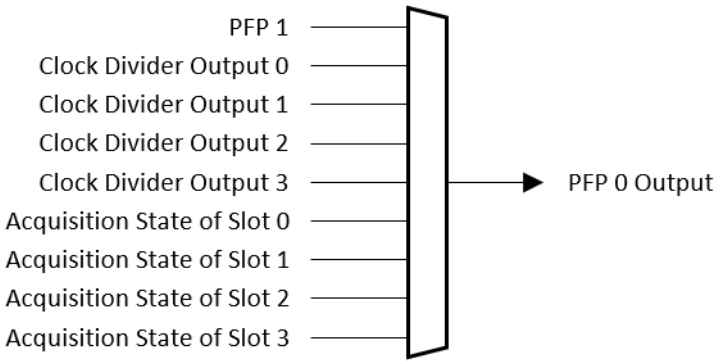


Figure 3.2 Signal routing for programmable function pin 0 as output.

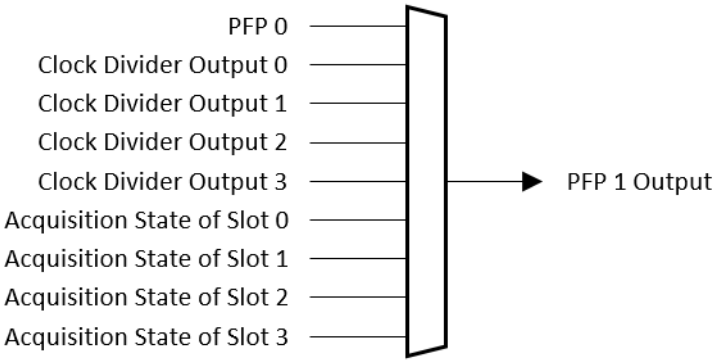


Figure 3.3 Signal routing for programmable function pin 1 as output.

3.3 Analog Input

Insert an iDAQ module supporting analog input function to perform analog input measurement. The following sections describe the analog input acquisition mechanism. For detailed specifications of the analog input functions, please refer to the document of the individual iDAQ module.

3.3.1 Instant Analog Input Acquisition

With instant analog input acquisition, the software controls the sample timing. The analog-to-digital converter (ADC) is continuously converting analog input signal by its maximum allowable conversion rate. Each time the software sends a “read instant analog input sample” command, the most recent conversion result is sampled as shown in Figure 3.4.

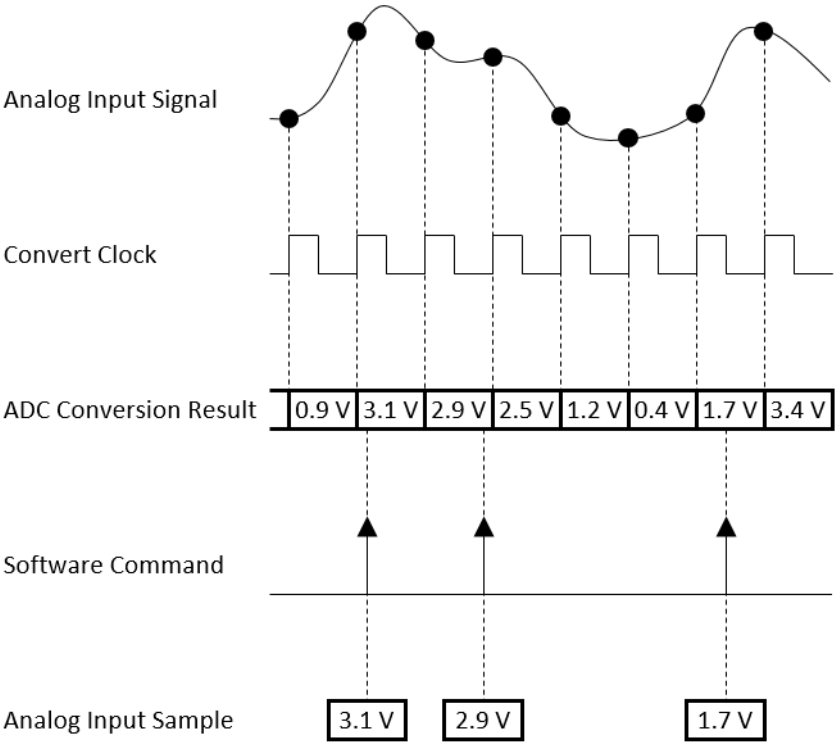


Figure 3.4 Instant analog input acquisition

3.3.2 Buffered Analog Input Acquisition

With buffered analog input acquisition, the ADC conversion rate and the duration of the acquisition is controlled by hardware timing signals. All conversion results are sampled and stored in the buffer memory before sending back to the host computer as shown in Figure 3.5.

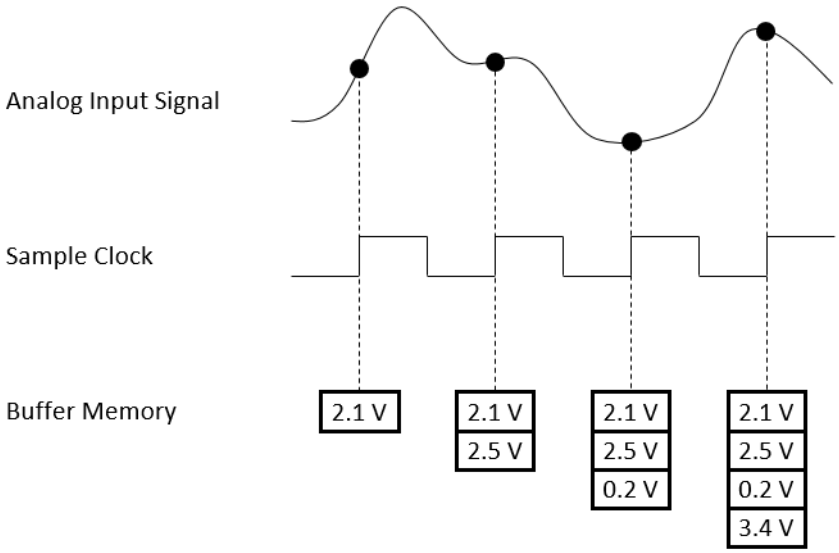


Figure 3.5 Buffered analog input acquisition

The start and stop of the acquisition are controlled by the start trigger and stop trigger, respectively. When configuration is completed, the acquisition engine of the iDAQ chassis is at standby state. After receiving a start trigger, acquisition becomes active and each rising edge of the sample clock acquires one analog input sample. The acquisition active period lasts until a stop trigger is received, which ends the acquisition. This is shown in Figure 3.6.

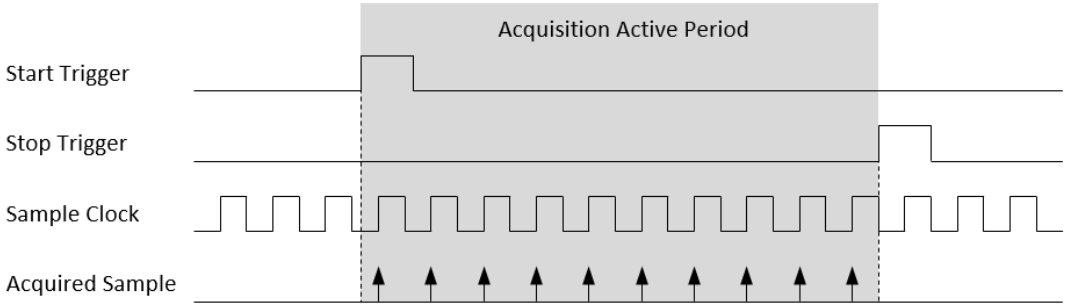


Figure 3.6 Start and stop of the analog input acquisition

The start and stop of acquisition can also be delayed in number of samples after receiving the corresponding trigger signal. As shown in Figure 3.7, the start of acquisition is delayed by 3 samples after receiving a start trigger, and the stop of acquisition is delayed by 2 samples after receiving a stop trigger.

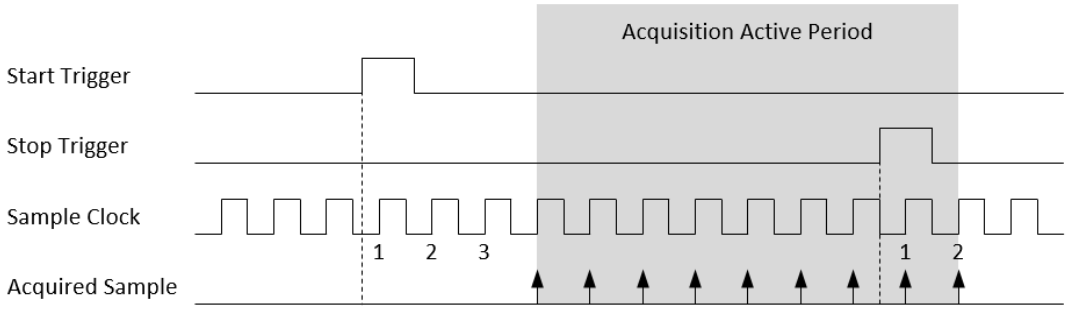


Figure 3.7 Start and stop of the analog input acquisition with delay

Refer to section 3.1.1 Trigger and Signal Routing for possible signal routings and configurations for these timing signals (start trigger, stop trigger, and sample clock).

Buffered analog input acquisition has several advantages over instant analog input acquisition:

- The start and stop time of acquisition (or duration of the acquisition) can be precisely controlled by hardware trigger signals.
- ADC conversion rate is configurable, and the sample rate can be much higher by using hardware sample clock signal.
- Time between samples is deterministic.

3.3.3 Analog Input Convert Clock Signal Behavior

While the frequency of the sample clock can be configured as a deterministic value, the convert clock of the ADC may present different behaviors in different types of analog input modules.

Multiplexed Analog Input Module

In a multiplexed analog input module, there is only one ADC performing conversion, which means only one channel at a time can be converted. An analog multiplexer (MUX) in front of the ADC routes the analog input channel to be converted to the ADC input as shown in Figure 3.8. Because the conversion time of the ADC remains the same, the maximum convert rate of the ADC will be shared by all enabled analog input channels. That is, if more analog input channels are enabled, the maximum allowable convert rate for each channel becomes smaller.

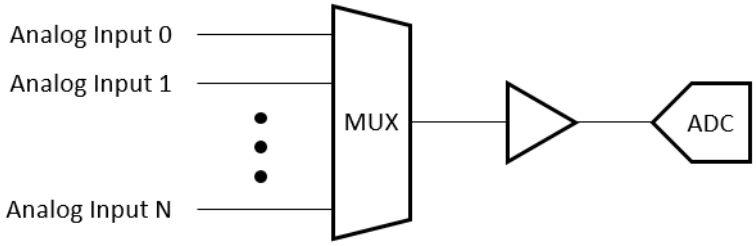


Figure 3.8 Multiplexed analog input module block diagram

When the sample clock rises, the multiplexed analog input module automatically generates required convert clocks using the maximum allowable convert clock rate of the ADC for all enabled channels. The MUX routes one of the enabled channels for each convert clock in the order of channel number. Figure 3.9 shows an example when 3 analog input channels (0, 1, and 2) are enabled. By this acquisition method, the timing of conversion for all enabled channels can be as close as possible, which approaches the result of a simultaneously sampled analog input module.

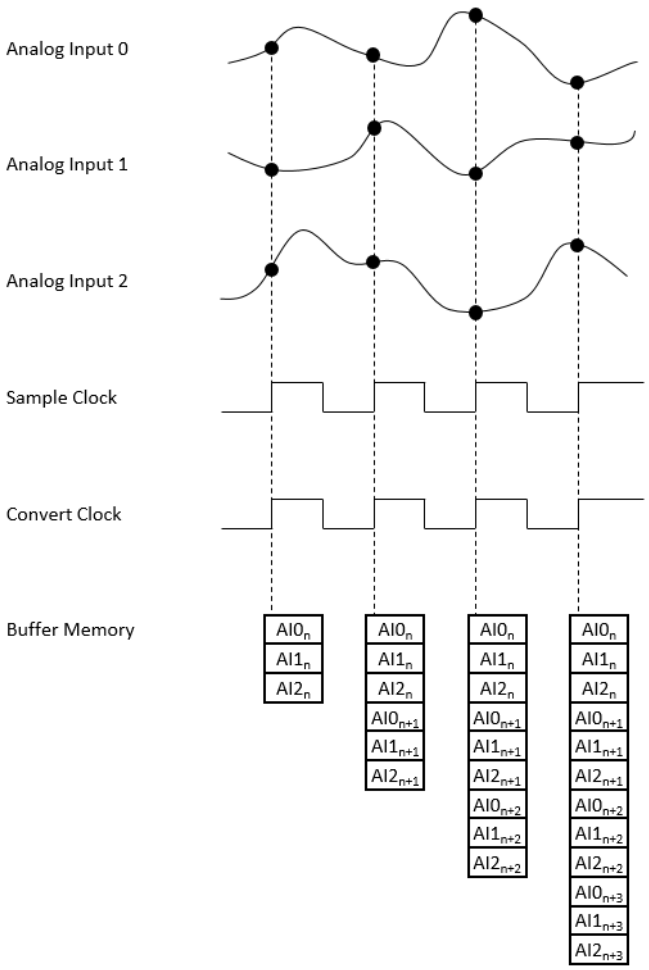


Figure 3.9 Acquisition of a multiplexed analog input module

Simultaneously Sampled Analog Input Module

In a simultaneously sampled analog input module, each analog input channel has its own ADC. When the sample clock rises, the ADC of all enabled channels start conversion simultaneously. The sampled results represent the analog input values at the same time. Figure 3.10 and Figure 3.11 show the block diagram and acquisition behavior of this kind of module.

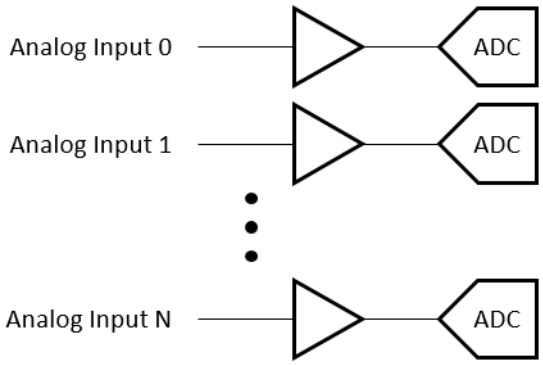


Figure 3.10 Simultaneously sampled analog input module block diagram

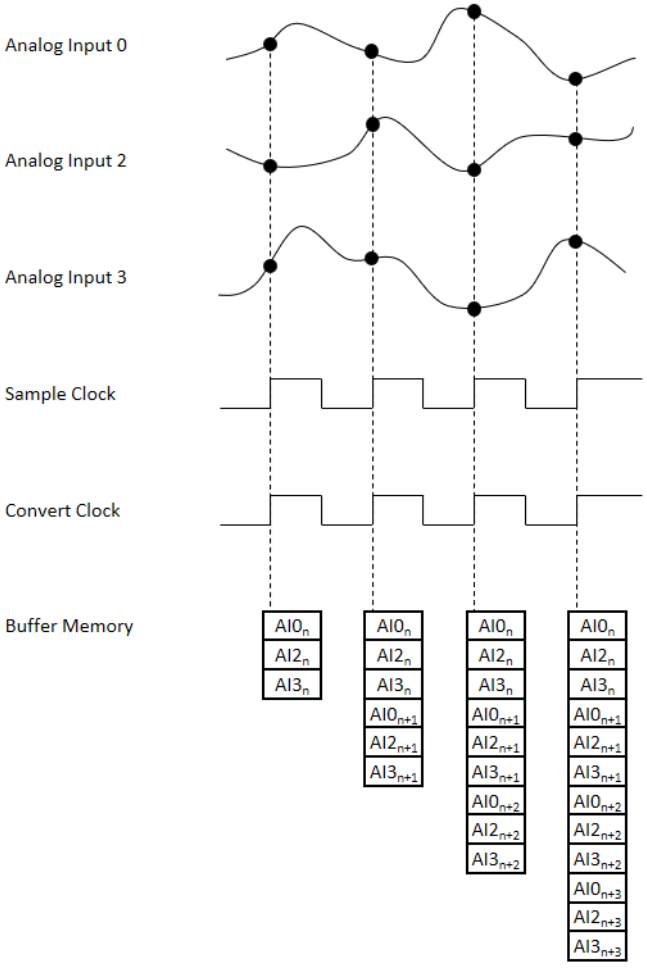


Figure 3.11 Acquisition of a simultaneously sampled analog input module

Sigma-Delta ADC Analog Input Module

Unlike the successive-approximation register (SAR) ADC, which performs one conversion for each convert clock, the sigma-delta ADC requires a continuous high-frequency oversample clock to perform the conversion. Therefore, this kind of modules cannot accept the sample clock from the programmable clock divider output of the chassis, programmable function pins, or signal of other slots as other types of analog input modules do.

The output data rate of a sigma-delta ADC analog input module is usually limited to several choices, such as

$$\frac{256\,kS/s}{N}$$

where N = 1, 2, 4, 8, … etc.

Before starting acquisition, a synchronization pulse will be sent to each sigma-delta ADC analog input modules to reset the ADCs at the same time. This synchronization pulse ensures that all sigma-delta ADCs will provide output data at the same time.

Due to the internal digital filter operation, the sigma-delta ADC module exhibits a fixed “input signal to output data” delay which is also called “group delay” compared to other types of analog input modules as shown in Figure 3.12. Refer to the specifications of the corresponding iDAQ module for the delay value.

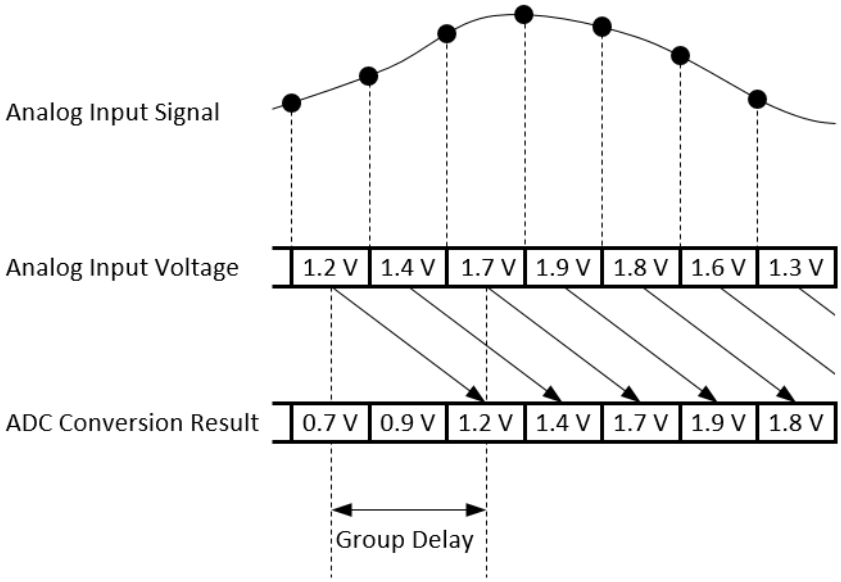


Figure 3.12 Group delay of the sigma-delta ADC analog input module

The sigma-delta ADC module can generate a data ready timing signal. This signal can be routed to other non-sigma-delta ADC type modules as their sample clock.

Low Conversion Rate ADC Analog Input Module

For iDAQ modules measuring slow varying signals such as temperature, strain, or pressure, the conversion rate of the ADC is usually accordingly slow. To prevent the sample rate from being limited to a low value due to this characteristic when synchronizing low conversion rate ADC analog input modules with other types of iDAQ modules, the sample rate of the module and conversion rate of the ADC are independently set.

If the sample rate is higher than the conversion rate, multiple samples from the same conversion result are provided. This is shown in Figure 3.13.

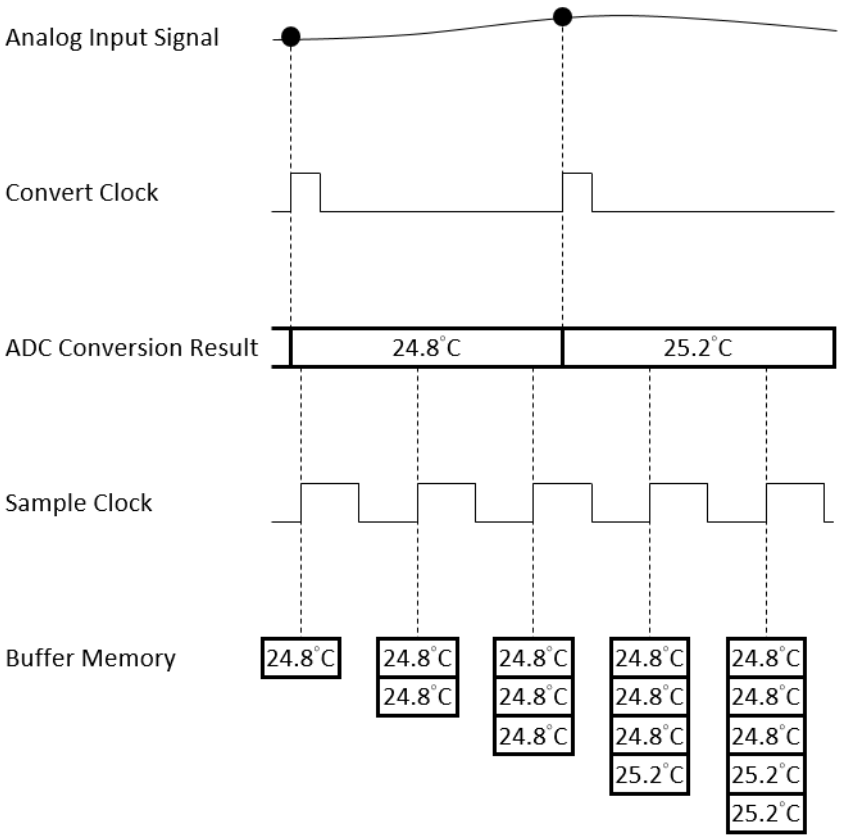


Figure 3.13 Acquisition of a low conversion rate ADC analog input module

3.3.4 Analog Comparison

Some of the analog input modules provide analog comparison function. The compare result can be routed to the chassis as a timing signal.

Analog comparison function compares one of the analog input signals to a preset threshold value. If the analog input signal is higher than the threshold value, result signal is high; otherwise, result signal is low. This is shown in Figure 3.14.

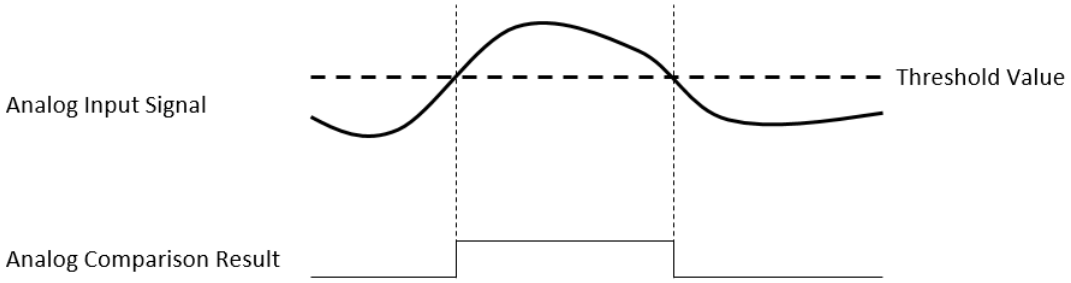


Figure 3.14 Analog comparison

To prevent a glitch of the analog comparison results due to noise in the analog input signals, hysteresis values can be added to the threshold value. With hysteresis values, analog comparison results becomes high only when analog input signal becomes higher than the upper threshold value; it becomes low only when analog input signal becomes lower than the lower threshold value - it remains unchanged otherwise.

Analog comparison can be selected as rising edge active or falling edge active. The upper and lower threshold values are different with different active edge settings. For rising edge active, the upper threshold value is equal to threshold value, and the lower threshold value is equal to threshold value minus hysteresis value, as shown in Figure 3.15. For falling edge active, the upper threshold value is equal to threshold value plus hysteresis value, and the lower threshold value is equal to threshold value, as shown in Figure 3.16.

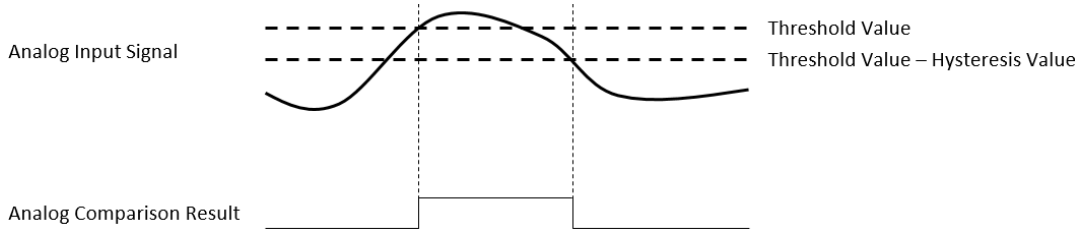


Figure 3.15 Analog comparison with hysteresis, rising edge active

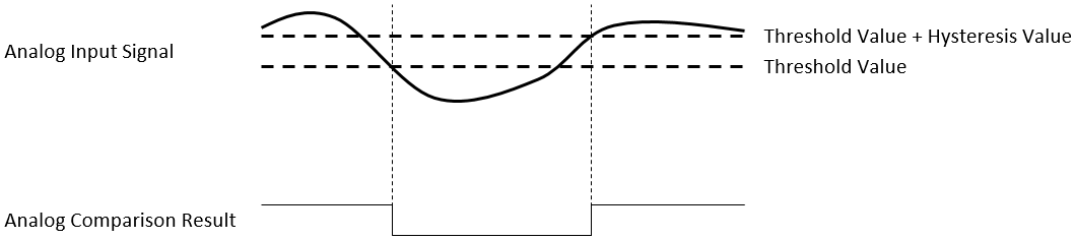


Figure 3.16 Analog comparison with hysteresis, falling edge active

3.4 Analog Output

Insert an iDAQ module supporting analog output function to perform analog output update/generation. The following sections describe the analog output update/generation mechanism. For detailed specifications of the functions, refer to the document of the corresponding iDAQ module.

3.4.1 Static Analog Output Update

With static analog output update, the analog output voltage or current is updated only when the software sends an “write static analog output sample” command. The analog output voltage or current remains unchanged at other times. This is shown in Figure 3.17.

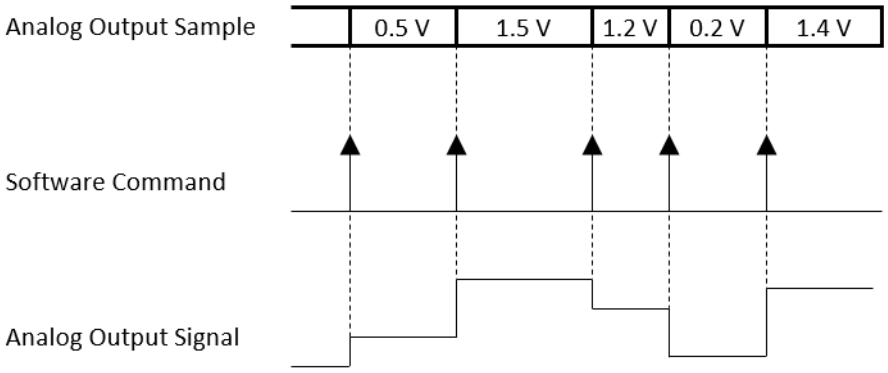


Figure 3.17 Static analog output update

3.4.2 Buffered Analog Output Waveform Generation

With buffered analog output waveform generation, the DAC conversion rate and the duration of the generation is controlled by hardware timing signals. The analog output waveform to be generated are first programmed and stored in the buffer memory in a digital form. The digital values are converted to analog voltage or current one by one for each sample clock as shown in Figure 3.18.

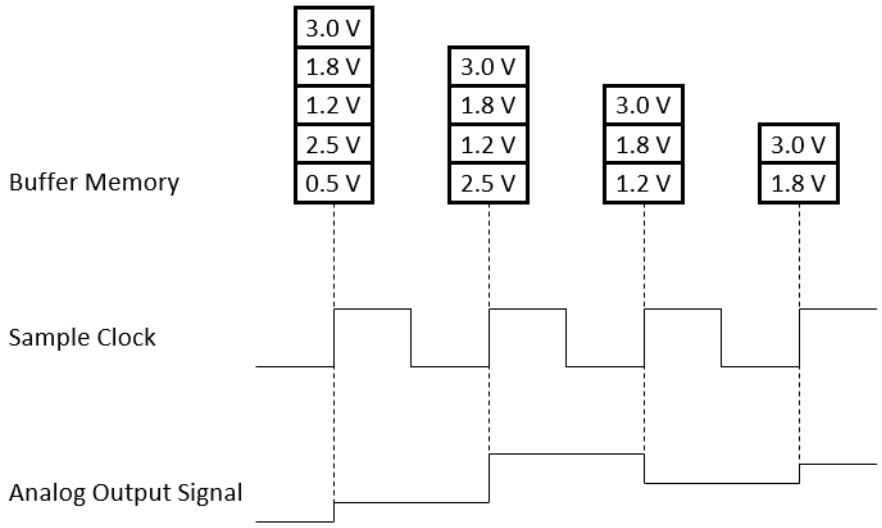


Figure 3.18 Buffered analog output waveform generation

The start and stop of the generation are controlled by the start trigger and stop trigger, respectively. When configuration is complete, the acquisition engine of the iDAQ chassis is at standby state. After receiving a start trigger, generation becomes active and each rising edge of the sample clock converts one analog output sample. The generation active period lasts until a stop trigger is received, which ends the generation. This is shown in Figure 3.19.

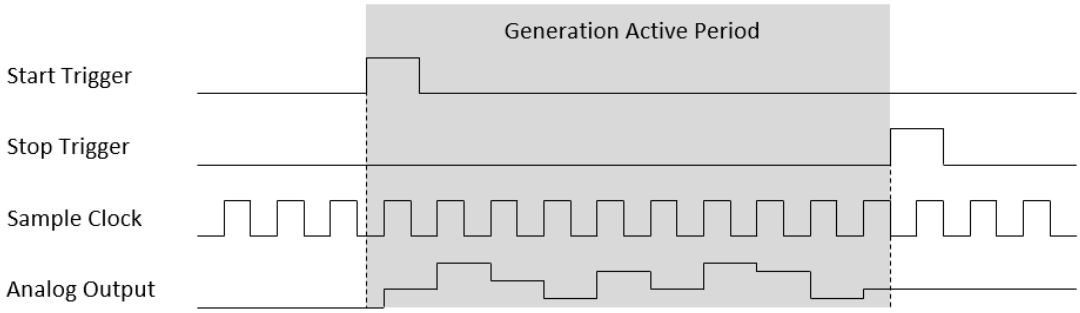


Figure 3.19 Start and stop of the analog output waveform generation

The start and stop of generation can also be delayed in number of samples after receiving the corresponding trigger signal. As shown in Figure 3.20, the start of generation is delayed by 3 samples after receiving a start trigger, and the stop of generation is delayed by 2 samples after receiving a stop trigger.

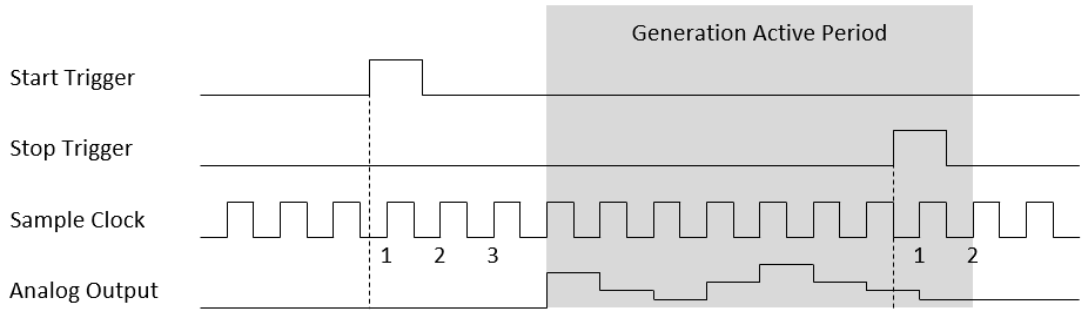


Figure 3.20 Start and stop of the analog output waveform generation with delay

Refer to 3.1.1 Signal Routing for possible signal routings and configurations for these timing signals (start trigger, stop trigger, and sample clock).

Buffered analog output waveform generation has several advantages over static analog output update:

- The start and stop time of generation (or duration of the generation) can be precisely controlled by hardware trigger signals.
- DAC conversion rate is configurable, and update rate can be much higher by using hardware sample clock signal.
- Time between samples is deterministic.

3.5 Digital Input

Insert an iDAQ module supporting digital input function to perform digital input measurement. The following sections describe the digital input acquisition mechanism. For detailed specifications of the functions, refer to the document of the corresponding iDAQ module.

3.5.1 Digital Input Functions

Digital Input Interrupt

All digital input channels can generate software interrupts (or events) to notice the application about the state change of input signals. Interrupts can occur at rising edge, falling edge, or both edges of the digital input signal as shown in Figure 3.21, Figure 3.22, and Figure 3.23, respectively. The enable/disable interrupt function and the selection of interrupt edges can be configured independently for each digital input channel.

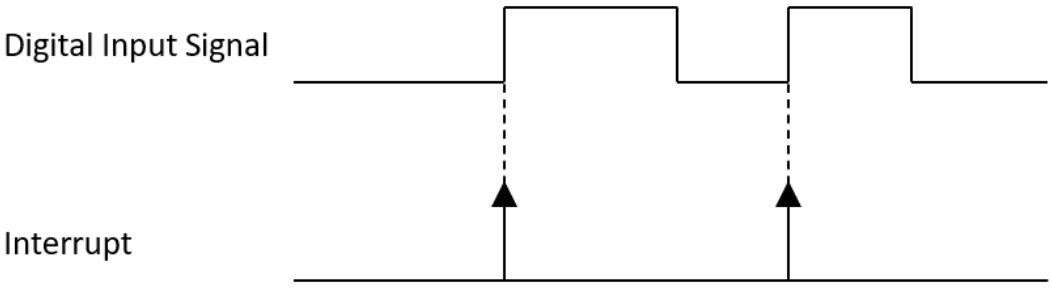


Figure 3.21 Digital input rising edge interrupts

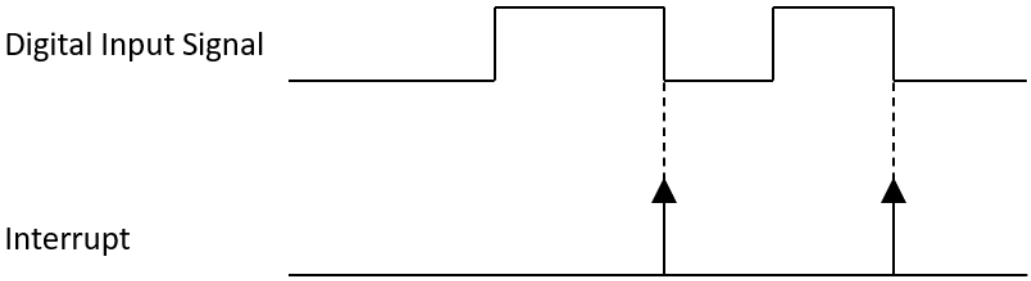


Figure 3.22 Digital input falling edge interrupts

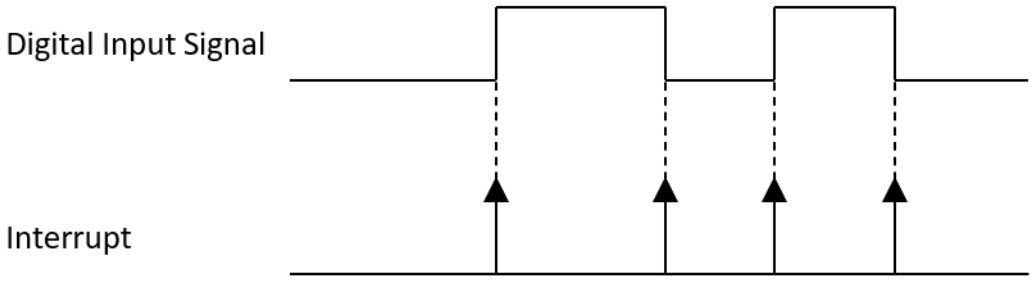


Figure 3.23 Digital input both edges interrupts

Digital Input Pattern Match Interrupt

Digital input channels can also generate an interrupt by detecting a specific pattern. The pattern can be configured by ports, and each channel can be enabled or disabled the detection independently. For example, if channels 0, 1, 2, 3, 6, and 7 of a digital input port is pattern match detect enabled, and the pattern is “10xx0100” (channel 7 through 0, where x indicates don’t care bit), the pattern match interrupt will be generated as shown in Figure 3.24.

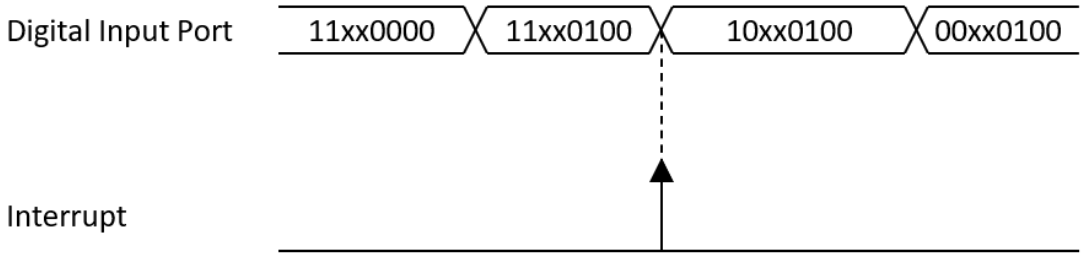


Figure 3.24 Digital input pattern match interrupt for pattern “10xx0100”

Digital Input Debounce Filter

To prevent false interrupts due to noise or bouncing in the signal, the digital input signals can be filtered. If digital input filter is enabled, transient signals with duration smaller than the filter duration will be considered as glitches and will not generate interrupts as shown in Figure 3.25. Digital input debounce filter can be enabled or disabled independently for each channel, and filter duration can be configured by ports (8 channels).

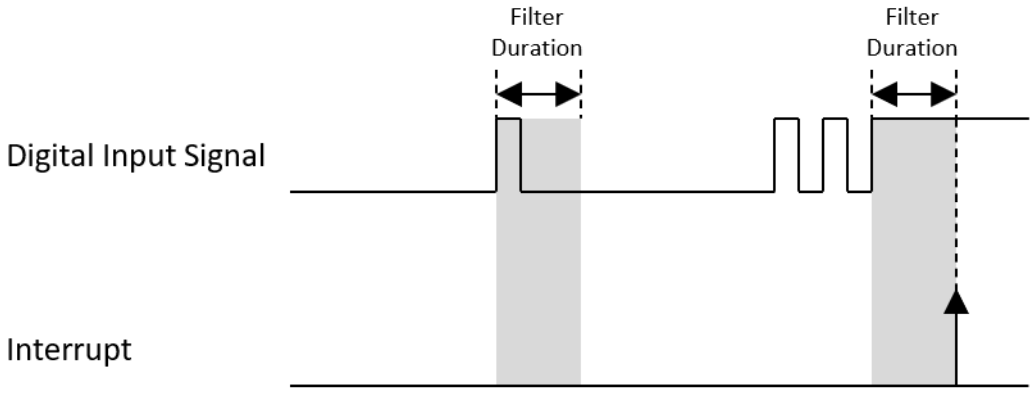


Figure 3.25 Digital input debounce filter

3.5.2 Instant Digital Input Acquisition

With instant digital input acquisition, the software controls the sample timing. Each time the software sends a “read instant digital input sample” command, the state of all digital input channels is sampled as shown in Figure 3.26.

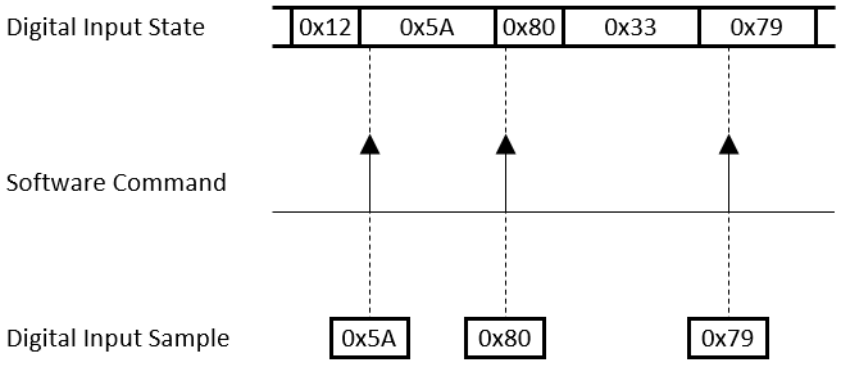


Figure 3.26 Instant digital input acquisition

3.5.3 Buffered Digital Input Acquisition

With buffered digital input acquisition, the sample rate and the duration of the acquisition is controlled by hardware timing signals. All samples are stored in the buffer memory before sending back to the host computer as shown in Figure 3.27.

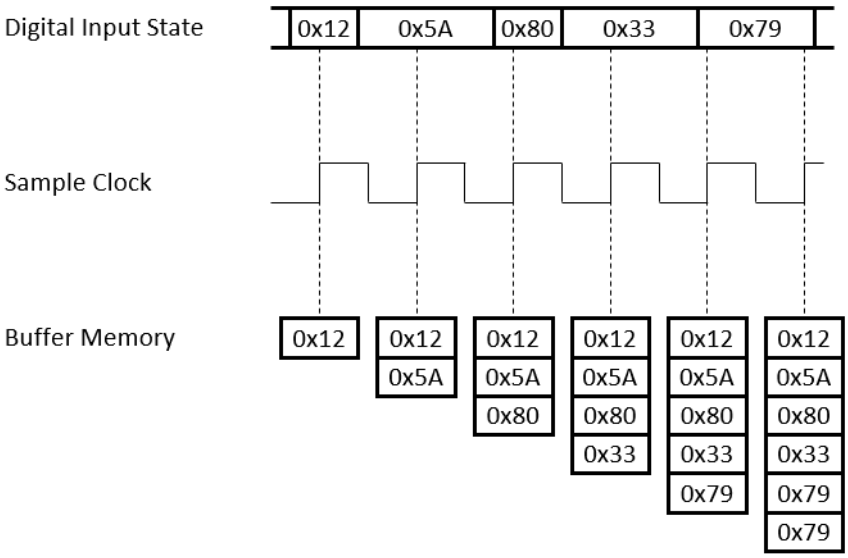


Figure 3.27 Buffered digital input acquisition

The start and stop of the acquisition are controlled by the start trigger and stop trigger, respectively. When configuration is completed, the acquisition engine of the iDAQ chassis is at standby state. After receiving a start trigger, acquisition becomes active and each rising edge of the sample clock acquires one analog input sample. The acquisition active period lasts until a stop trigger is received, which ends the acquisition. This is shown in Figure 3.28.

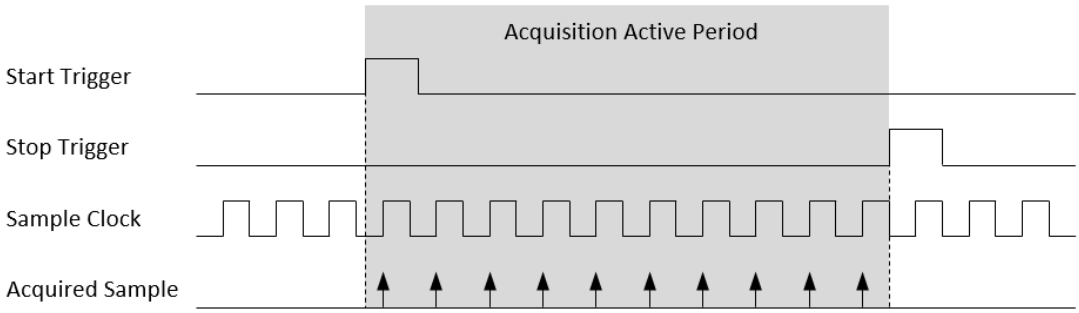


Figure 3.28 Start and stop of the digital input acquisition

The start and stop of acquisition can also be delayed in number of samples after receiving the corresponding trigger signal. As shown in Figure 3.29, the start of acquisition is delayed by 3 samples after receiving a start trigger, and the stop of acquisition is delayed by 2 samples after receiving a stop trigger.

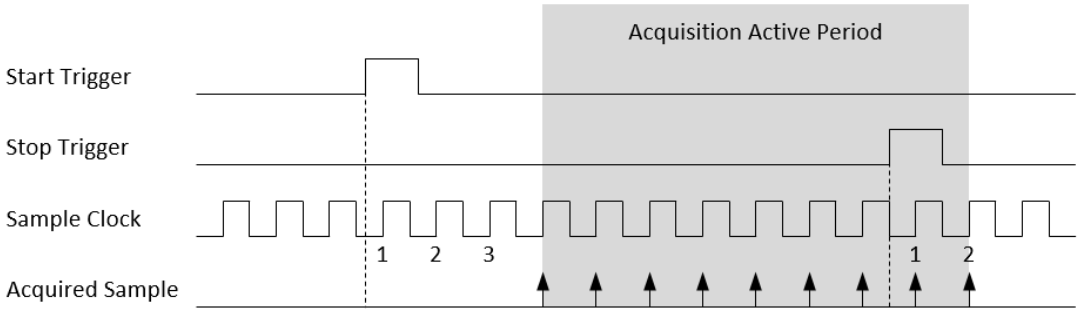


Figure 3.29 Start and stop of the digital input acquisition with delay

Refer to 3.1.1 Signal Routing for possible signal routings and configurations for these timing signals (start trigger, stop trigger, and sample clock).

Buffered digital input acquisition has several advantages over instant digital input acquisition:

- The start and stop time of acquisition (or duration of the acquisition) can be precisely controlled by hardware trigger signals.
- Sample rate can be much higher by using hardware sample clock signal.
- Time between samples is deterministic.

3.6 Digital Output

Insert an iDAQ module supporting digital output function to perform digital output update/generation. The following sections describe the digital output update/generation mechanism. For detailed specifications of the functions, refer to the document of the corresponding iDAQ module.

3.6.1 Static Digital Output Update

With static digital output update, the digital output state is updated only when the software sends an “write static digital output sample” command. The digital output state remains unchanged at other times. This is shown in Figure 3.30.

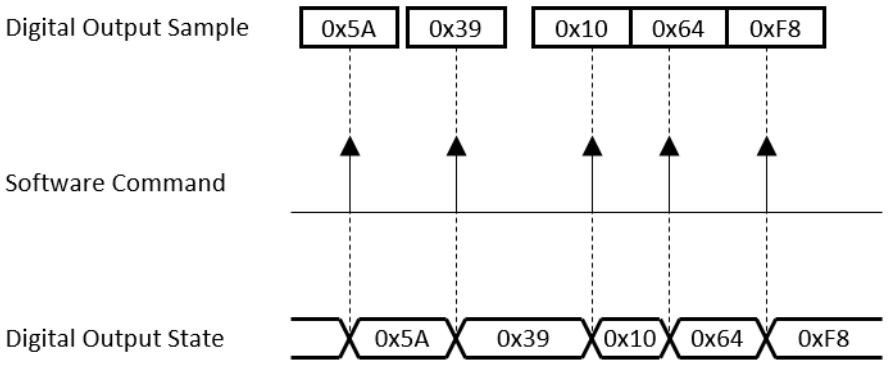


Figure 3.30 Static digital output update

3.6.2 Buffered Digital Output Waveform Generation

With buffered digital output waveform generation, the rate and duration of the generation is controlled by hardware timing signals. The digital output waveform to be generated are first programmed and stored in the buffer memory. The digital output state then is updated for each sample clock as shown in Figure 3.31.

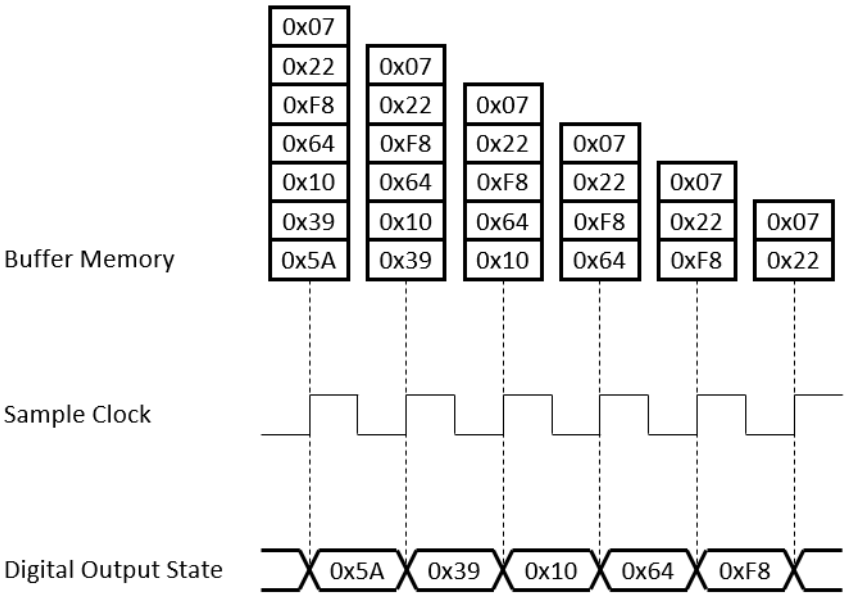


Figure 3.31 Buffered digital output waveform generation

The start and stop of the generation are controlled by the start trigger and stop trigger, respectively. When configuration is completed, the acquisition engine of the iDAQ chassis is at standby state. After receiving a start trigger, generation becomes active and each rising edge of the sample clock converts one analog output sample. The generation active period lasts until a stop trigger is received, which ends the generation. This is shown in Figure 3.32.

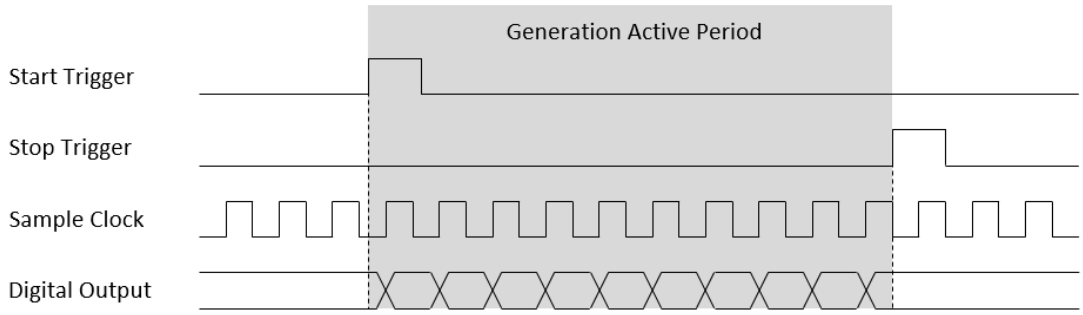


Figure 3.32 Start and stop of the digital output waveform generation

The start and stop of generation can also be delayed in number of samples after receiving the corresponding trigger signal. As shown in Figure 3.33, the start of generation is delayed by 3 samples after receiving a start trigger, and the stop of generation is delayed by 2 samples after receiving a stop trigger.

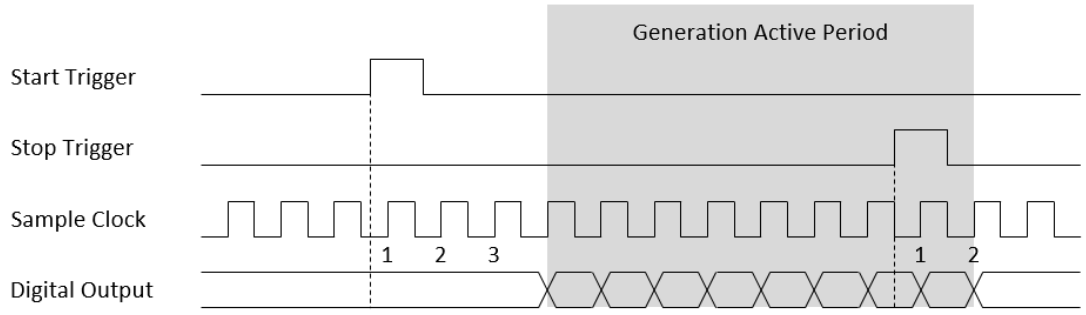


Figure 3.33 Start and stop of the digital output waveform generation with delay

Refer to 3.1.1 Signal Routing for possible signal routings and configurations for these timing signals (start trigger, stop trigger, and sample clock).

Buffered digital output waveform generation has several advantages over static digital output update:

- The start and stop time of generation (or duration of the generation) can be precisely controlled by hardware trigger signals.
- Update rate can be much higher by using hardware sample clock signal.
- Time between samples is deterministic.

3.7 Status Indication

The LED indicates the chassis status. Please refer to below table for the status indication with respective color state.

LED	LED Color		
	Green	**Yellow**	**Off**
PWR	Power on	---	No power
LINK	Upstream is connected to SuperSpeed (5 Gb/s)	Upstream is connected to High-Speed (480 Mb/s)	Upstream is not connected or suspended
ACT	Upstream traffic present	---	No upstream traffic present

3.8 Device Description

The Device Description is used to differentiate the modules in the iDAQ system. It's given following a naming rule of combining chassis ID, model name and slot number. You can change the description in Navigator, or just leave it as default. The description is used in your own program, in order to get control or device handler from the device.

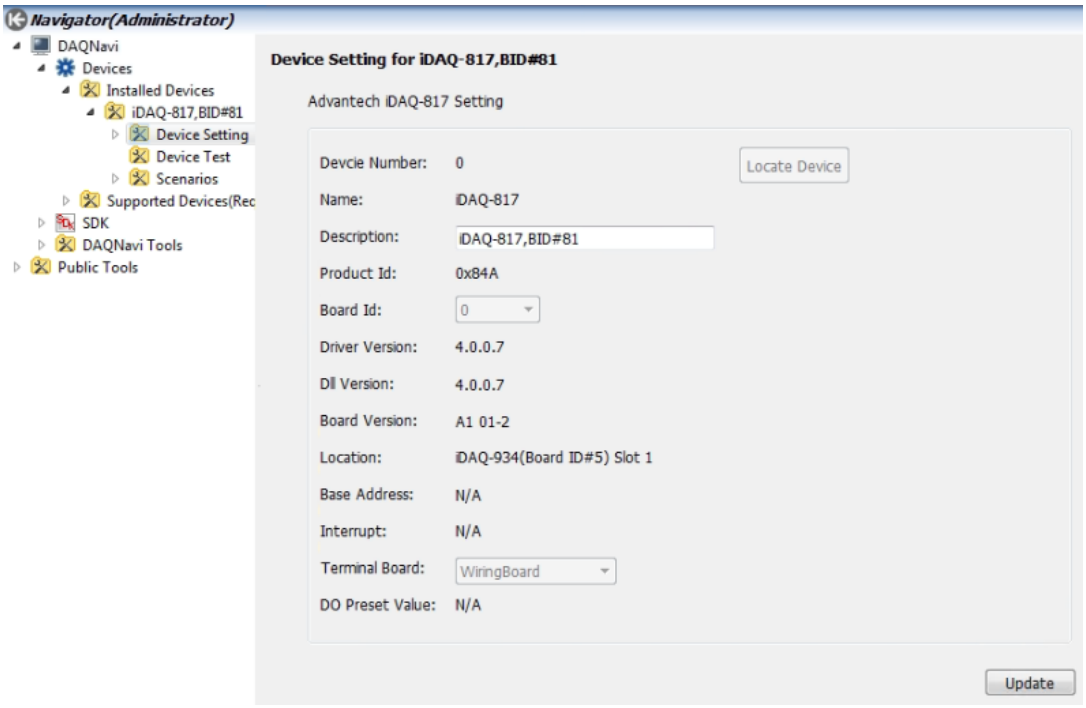


Figure 3.34 Device description shown in Navigator

The rotary switch and the its corresponded number can be found in below table.

Switch Position	Chassis ID	Switch Position	Chassis ID
0	0	8	8
1	1	9	9
2	2	A	10
3	3	B	11
4	4	C	12
5	5	D	13
6	6	E	14
7	7	F	15

Appendix A

Specifications

A.1 Analog Input

Please refer to the specifications of individual iDAQ analog input module.

A.2 Analog Output

Please refer to the specifications of individual iDAQ analog output module.

A.3 Digital Input

Please refer to the specifications of individual iDAQ digital input module.

A.4 Digital Output

Please refer to the specifications of individual iDAQ digital output module.

A.5 Counter

Please refer to the specifications of individual iDAQ counter module.

A.6 Programmable Function Pins (PFP)

- Channels: BNC x 2
- Direction: Input or output, software configurable
- Input level
  - Logic high: +3.5 V min.
  - Logic low: +1.5 V max.
- Input protection voltage: +6.5 V max, -0.5 V min.
- Pull-down resistor: 10 kΩ
- Input signal frequency: 10 MHz max.
- Response time: 20 ns max.
- Debounce filter: 40 ns ~ 168 ms, software configurable
- Output logic level
- Logic high: +4.5 V min., 20 mA source max.
- Logic low: +0.5 V max., 20 mA sink max.

A.7 General

iDAQ-934:

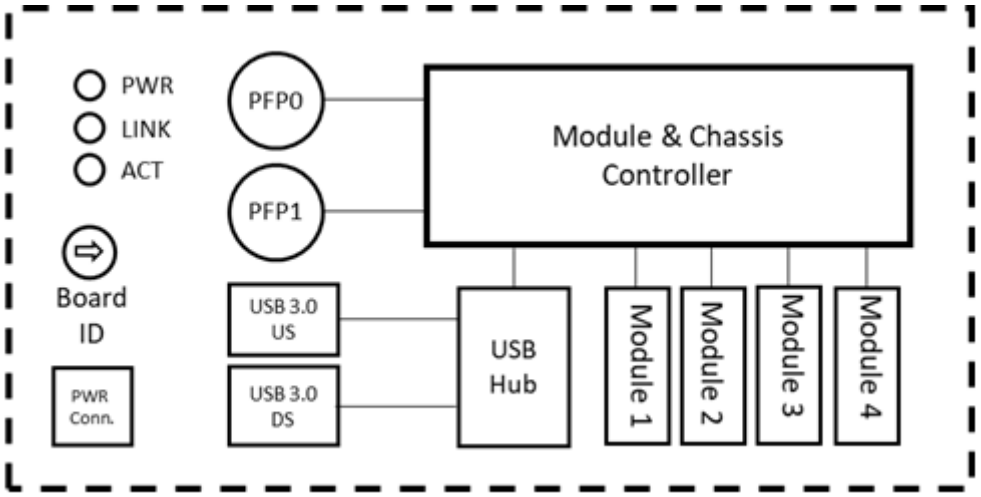
- Interface: SuperSpeed USB 3.0
- Data transfer rate: 5 Gbps max.
- USB downstream port: 1 port
- Power Input: 10 ~ 30 V_{DC}
- Power Consumption: 24 W max., including modules and USB downstream port loads
- Power consumption from USB: 100 µA max.
- Power connector: 2-pin spring terminal
- Module dimensions: 178 x 100 x 71 mm (7.01 x 3.93 x 2.80 in.)
- Operating temperature: -20 °C to 60 °C (-4 °F to 140 °F)
- Storage temperature: -40 °C to 70 °C (-40 °F to 158 °F)
- Operating humidity: 10% to 90% RH, non-condensing
- Storage humidity: 5% to 95% RH, non-condensing
- Vibration: $5G_{rms}$, random, 5~500Hz, 1hr/axis
- Shock: 30G, half sine, 11ms

iDAQ-964:

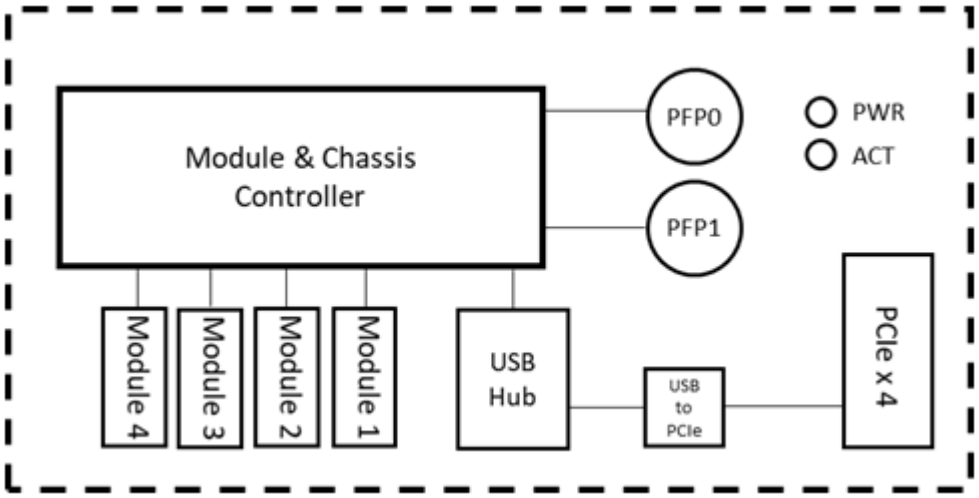
- Power Input: 3.3V and 12V, through PCI Express BUS (AMAX-5000 series)
- Power Consumption: 24 W max., including modules
- Module dimensions: 139.5 x 84.2 x 100 mm (5.49" x 3.31" x 3.94")
- Operating temperature: -10 to 60° C (-4 to 140° F) @ 5 to 85% RH with 0.7m/s airflow
- Storage temperature: -40 to 85° C (-40 to 185° F)
- Operating humidity: 95% RH @ 40° C, non-condensing
- Shock: 10G, half sine, 11 ms
- Vibration: 1 Grms, random, 5 ~ 500 Hz, 1hr/axis

A.8 Function Block

iDAQ-934



iDAQ-964

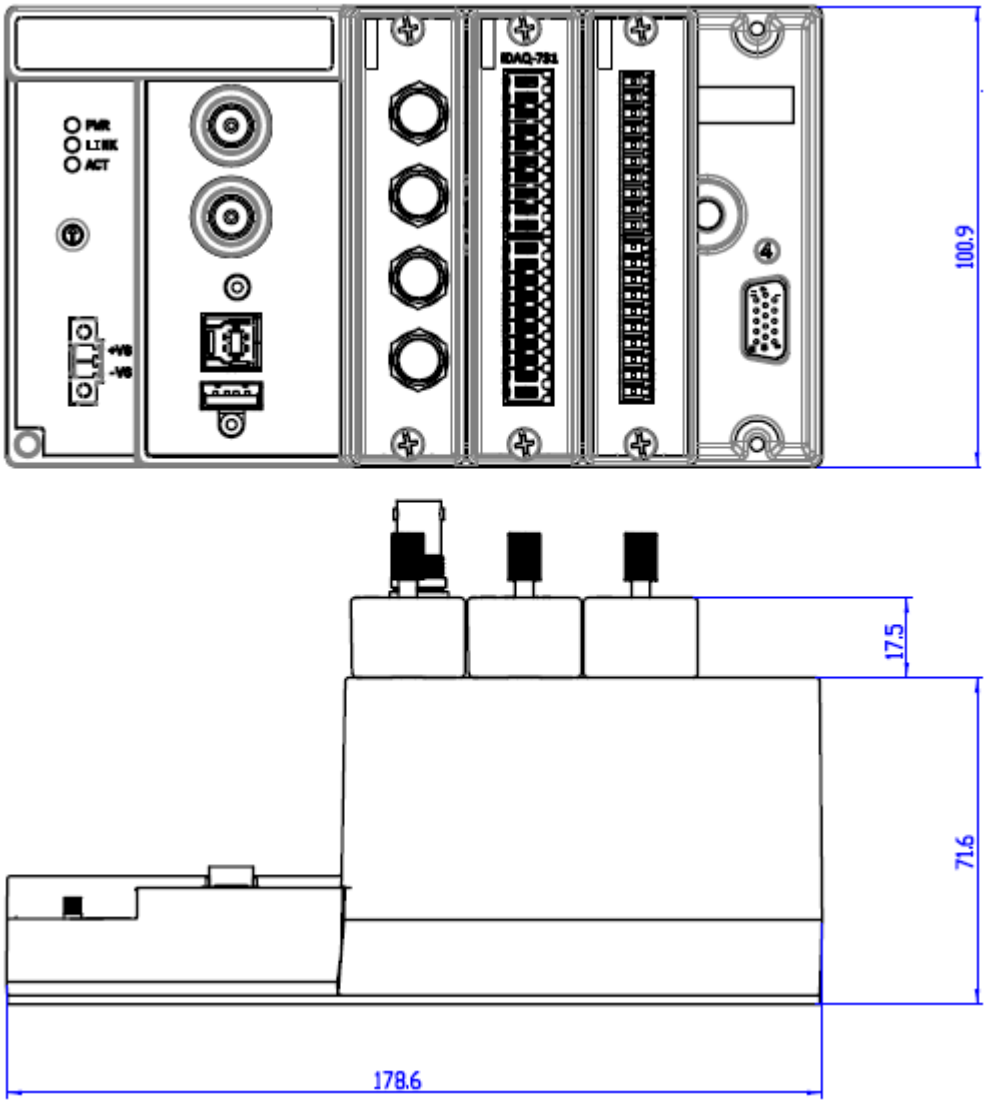


Appendix B

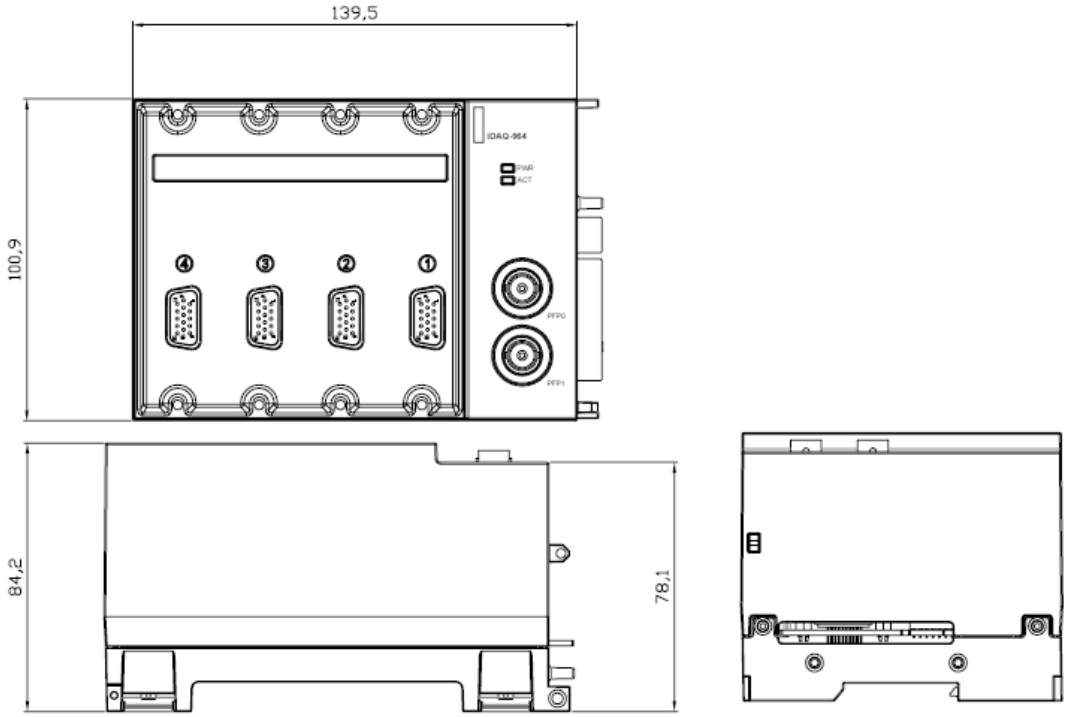
System Dimensions

B.1 Chassis

iDAQ-934

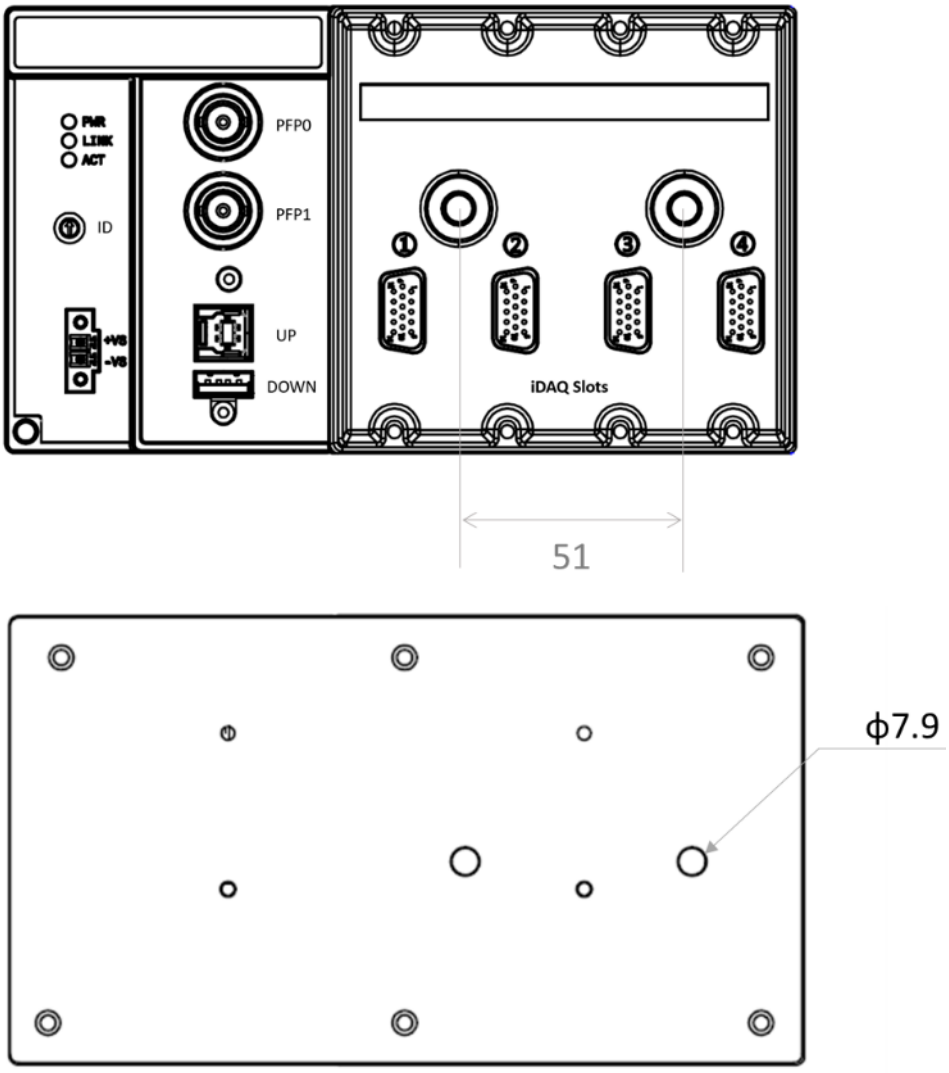


iDAQ-964



B.2 Mounting

Wall Mount for iDAQ-934



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